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Harmonic Rejection Mixers for Wideband Receivers

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Harmonic Rejection Mixers for Wideband Receivers

by

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DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

May 2013

To my daughters, Ni'mah and Tasneem

Acknowledgments

I would like to thank those without whom this work would not have been possible.

First, I would like to thank Tyson Tuttle of Silicon Labs for the generous support of this Ph.D. and for being a source of inspiration. I have been fortunate enough to have worked for Silicon Labs for the last 13 years. Though I had a master's degree at the time of joining Silicon Labs, a significant portion of my real-world engineering education happened while working in Tyson's group. I have learnt immensely by observing him and thank him for the mentorship and guidance I have received over the last several years. Working in his group definitely made me better as an engineer. I would also like to thank Alessandro Piovaccari of Silicon Labs. He diligently reviewed all publications involved in this dissertation and provided valuable feedback in a timely manner, despite the busy schedule he had as the Vice President of Engineering. I also thank him for his camaraderie that made the difficult times more bearable.

I'd like to thank my advisor, Dr. T. R. Viswanathan. Over the last four years that I have worked with him, he has been a continuous source of new insights. T.R.'s extensive experience in both industry and academia spanning several decades, provided me with valuable perspectives on technology and its

evolutionary trends. T.R. is also one of the best teachers that I have ever come across. His teaching style similar to story-telling is something I would like to emulate, if I get to teach some day. I thank him for this inspiration. I'd also like to thank my co-advisor, Dr. Hassibi, for the many suggestions he had given to enhance this dissertation. He always found time despite his busy schedule, and I thank him for his guidance and co-operation. I'd also like to thank my colleague and committee member, Dr. Shouli Yan for giving me several valuable inputs on writing a good dissertation. He took the time to review my dissertation and provided numerous useful suggestions. I thank him for his guidance.

I thank my committee members, Dr. Lizy John, Dr. Sriram Vishwanath and Dr. Nan Sun for taking the time to attend my Qualifying examination and Defense. Their suggestions for improvement greatly enhanced this dissertation.

Last but not the least, thanks are due to my wife, Shaista. During the course of this PhD we were blessed with our second daughter Tasneem. As parents of little kids know, managing little kids is a difficult task. As I was working weekends and nights on my dissertation, my wife kept the home fires burning. Even when I returned home late at night, she always greeted me with a smile. I thank her for taking care of the family and keeping a cheerful atmosphere at home during the last four years. Finally, I thank my sister, Salma Rafi, and my parents, for the motivation and encouragement they have provided me since I was a kid. My parents have been the driving force behind

all my educational endeavors. I thank them for re-kindling my motivation to complete this degree every time I was less inclined to do so.

Harmonic Rejection Mixers for Wideband Receivers

Publication No. _____

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The University of Texas at Austin, 2013

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This dissertation presents novel Harmonic Rejection (HR) Mixer architectures to obtain a high level of harmonic rejection. This is achieved by reducing the sensitivity to mismatches in devices operating at high frequencies. Consequently, the HR performance for this mixer architecture is primarily determined by resistor and capacitor matching at low intermediate frequencies (IF). Since large resistor areas can be used at relatively less power penalty in the low frequency IF section, superior HR performance is realized. A design fabricated in 110 nm CMOS process, rejects up to the first 14 local oscillator (LO) harmonics and achieves 3^{rd}, 5^{th} and 7^{th} HR ratios in excess of 52, 54 and 55 dB respectively, without any calibration or trimming. This mixer architecture also rejects flicker noise, has improved image rejection (IR) and second-order input-intercept-point (IIP2) performance. By using a clock N

times the desired LO frequency, this scheme rejects the $(N-1)^{th}$ LO harmonic only by an amount of $20log(N-1)$ dB. A new technique is presented that enables better HR for the $(N-1)^{th}$ harmonic while preserving the level of rejection for other harmonics. This mixer fabricated in 55 nm standard CMOS process has a programmable number of 8, 10, 12 or 14 mixer phases and achieves an improvement of 29 dB for the $(N-1)^{th}$ harmonic while achieving 52 dB of rejection for the 3^{rd} harmonic. It also rejects flicker noise and has an IIP2 performance of 68 dBm. The mixers presented in this dissertation set the state-of-the-art in HR performance for single-stage mixers with configurable number of phases without using any calibration or trimming.

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Chapter 1

Introduction

Wideband Receivers have gained increased attention from the industry and academia in the last five years. This has been fueled by the explosive consumer demand for flat-screen televisions across the world. Receiver architectures used in older TVs have implementations that are expensive, consume high power and require a large number of discrete components. The new consumer demand has driven the need to find low-cost solutions for a wideband receiver front-end without compromising the performance. This thesis addresses the main challenges in realizing a low-cost solution for a wideband receiver, focusing on the analog front end.

Section 1.1 presents an overview of the terrestrial and cable TV systems used in the different regions of the world. In section 1.2, a conventional receiver architecture is presented. Section 1.3 discusses the reason for the use of square-wave mixers for frequency translation in traditional CMOS receivers. The problem of harmonic rejection in a conventional receiver architecture is discussed in section 1.4. Section 1.5 discuses the existing approaches to address the harmonic rejection problem and in section 1.8, an overview of this dissertation's organization is presented.

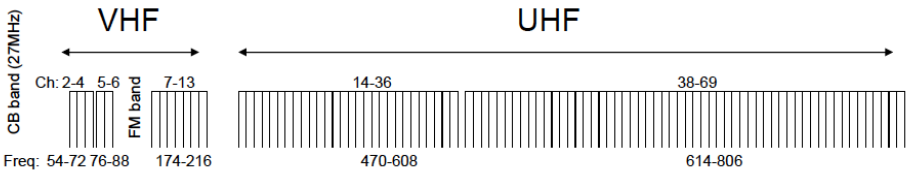


Figure 1.1: US Terrestrial TV Frequency Plan

1.1 A Wideband System: Television

Television is a wideband system with the carrier frequencies ranging from 50 MHz to 1 GHz. There are two broad classes of application for a TV receiver: 1) Terrestrial Television 2) Cable Television. Each of the two can further be classified into analog and digital modes based on the type of modulation used. Specifications come from different institutions in different geographical regions and most often are outdated by de-facto standard requirements. This is especially true in the case of analog TV for which a well established tradition of design and testing exists.

1.1.1 Terrestrial TV

The digital terrestrial transmissions in the US, Europe and Japan follow ATSC (Advanced Television Systems Committee) [11], ISDB (Integrated Services Digital Broadcasting) and DVB (Digital Video Broadcasting) standards. In the US, the RF spectrum from 54-88 MHz, 174-216 MHz and 470-806 MHz is used for transmission (1.1). The bands 54-88 MHz and 174-216 MHz are called the VHF (Very High Frequency) bands and 470-806 MHz is called UHF band (Ultra High Frequency). ATSC specifies a channel bandwidth of 6 MHz

Country	USA	Europe	Japan
System	ATSC	DVB-T	ISDB-T
Frequencies (MHz)	54-88, 174-216, 470-806	174-230, 470-862	470-770
Channel Bandwidth (MHz)	6	6, 7, 8	6
Modulation	8-VSB	OFDM (QPSK,16/64 QAM)	OFDM (QPSK,16/64 QAM)

Table 1.1: Digital Terrestrial Standards in the world

and uses 8-VSB modulation. The frequency plan for US is shown in shown in Fig. 1.1. Of the digital TV standards, ATSC imposes the toughest interferer profile peaking at 57 dBc for signal located 6 channels away from the desired channel [11].

Europe uses the DVB system. DVB is a family of video broadcast formats that encompasses terrestrial (DVB-T, T2), handheld (DVB-H), cable (DVB-C, C2) and satellite (DVB-S, S2, SH) [12]. DVB tuner specifications are mostly set by MBRAI [13, 14]. For terrestrial television, the frequencies from 174-230 MHz and 470-862 MHz are used. The channel bandwidth can be 6, 7 or 8 MHz. Orthogonal frequency division multiplexing (OFDM) with QPSK or 16/64 QAM is used as modulation. The digital terrestrial TV systems for different geographical regions in the world are summarized in Table 1.1.

Even though analog TV transmission has been phased out here, there are regions in the world that still use analog transmissions. Analog TV has the most stringent SNR requirements that can be higher than 40 dB [15, 16].

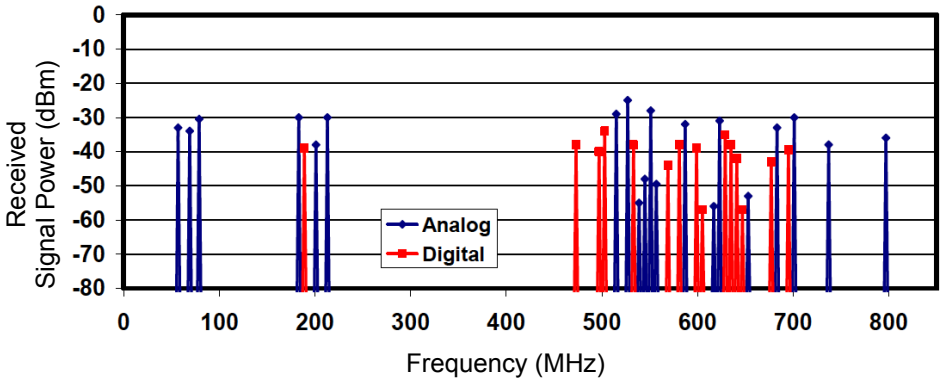


Figure 1.2: An example TV Spectrum [1].

An example signal profile at the input of a terrestrial TV [1] antenna is shown in Fig. 1.2. In addition to the TV signals shown in this figure, there can be out-of-band interferers at the antenna due to FM broadcast towers (76-108 MHz), mobile communications transmitters (850 MHz, 900 MHz, 1800 MHz, 1900 MHz and 2100 MHz), Bluetooth and WiFi (2.4 GHz) as shown in Fig. 1.3. These add further challenges to the design of a wideband receivers. While it is conceivable that these out-of-band interferers can be removed by using notch filters at the specific interferer frequency, this adds significantly to the system cost as there are several out-of-band interferers present. Performance is also degraded because the insertion loss of these filters worsens the noise figure of the receiver.

1.1.2 Cable TV

In contrast to terrestrial, the input spectrum for cable TV is continuously loaded with TV signals from 54 MHz to 1002 MHz (in the US as shown

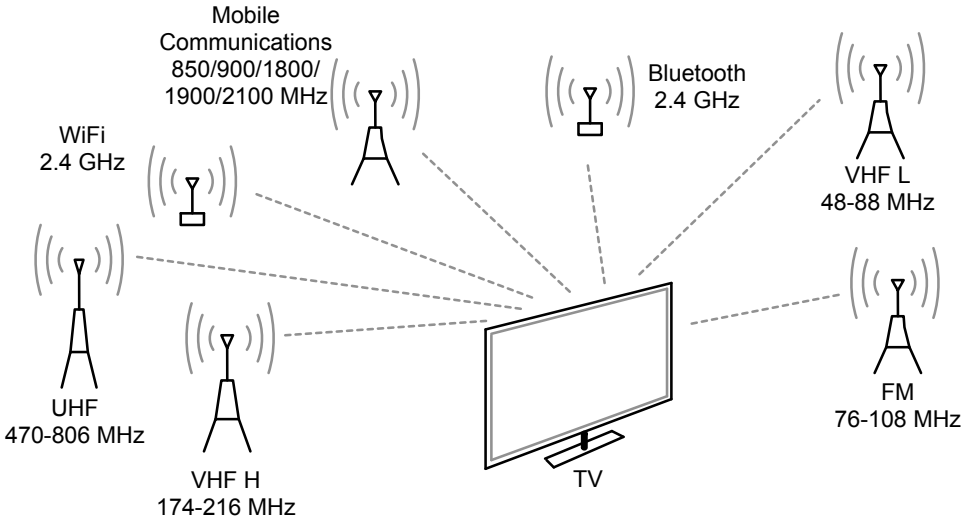


Figure 1.3: Signals present at the antenna of a TV.

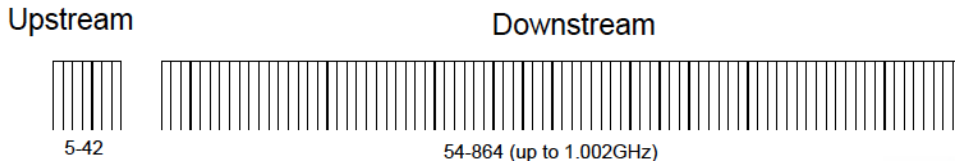


Figure 1.4: US cable TV Frequency Plan

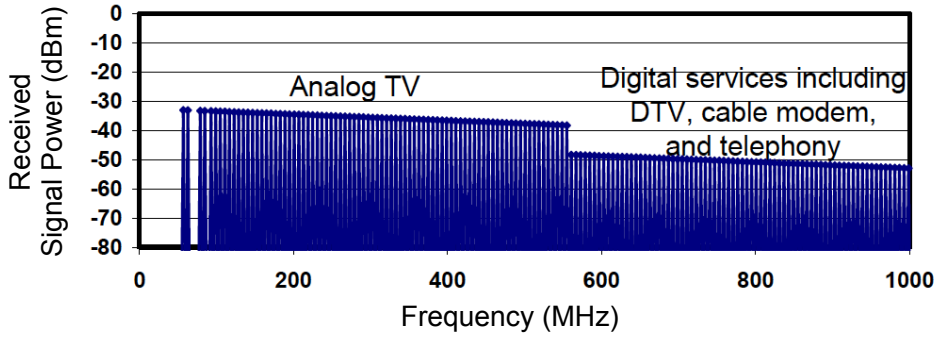


Figure 1.5: An example cable TV Spectrum [1].

Country	USA	Japan	Europe
System	OpenCable	ISDB-C	DVB-C
Frequencies (MHz)	54-806	90-770	47-862
Channel Bandwidth (MHz)	6	6	8
Modulation	64/256-QAM	64 QAM	16/32/64/128/256 QAM

Table 1.2: Cable TV Summary

in Fig. 1.4). The blocking profile is less demanding than ATSC with analog and digital interferers +18 and +15 dBc respectively for 64 QAM scheme. However very large number of channels populate the cable spectrum leading to tough linearity requirements. An example signal profile at the F-connector for cable TV is shown in Fig. 1.5.

Cable transmission operates on 6 MHz channel bandwidths in the US and Japan and uses QAM [17–20]. Europe uses DVB-C with 8 MHz channel bandwidths. 16/32/64/128/256 QAM is used here [12]. A high SNR of 33 dB is needed for 256 QAM. The US and Japan follow the openCable [19] and ISDB-C systems. The worldwide cable TV systems are summarized in Table 1.2.

1.2 Typical Receiver Architecture

In a typical receiver (Fig. 1.6), the wideband signal from the antenna is passed through an RF filter to reduce the level of interferers. After amplifi-

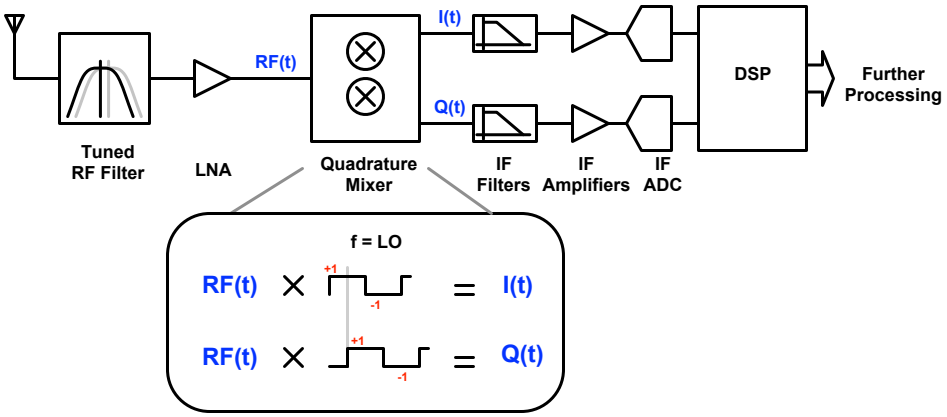


Figure 1.6: A typical receiver architecture.

cation though a low noise amplifier (LNA), the wanted RF signal is frequency translated to a lower intermediate-frequency (IF) by a quadrature mixer. The low-frequency IF signal is further filtered, amplified and digitized. Frequency translation to a lower frequency reduces the power consumed in the selective amplification of the wanted signal. Digitization enables the use of more complicated signal processing algorithms to efficiently demodulate and recover the message signal. This is particularly true in the light of the advances in CMOS technology where implementing signal processing functions digitally is less expensive and consumes lower power. Hence, frequency translation is an important step in the processing of the wanted signal.

Frequency translation is accomplished simply by multiplying the RF signal with a square-wave between ± 1 at a frequency of the local oscillator (LO) as shown in Fig. 1.6. Quadrature outputs, $I(t)$ and $Q(t)$, that have a phase shift of 90^o between them, are obtained by multiplying the RF signal

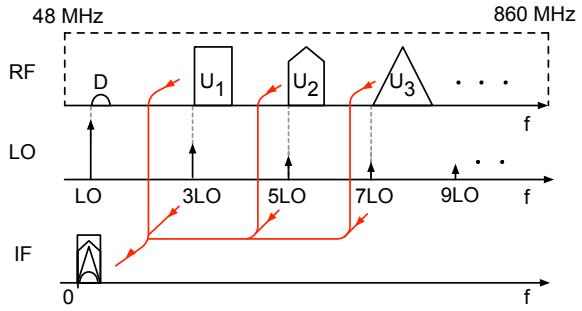
with time-shifted LO signals as shown. A quadrature mixer is used as it helps reduce corruption of desired signal from interferers at the image frequency [21].

1.3 Why Square-Wave mixers?

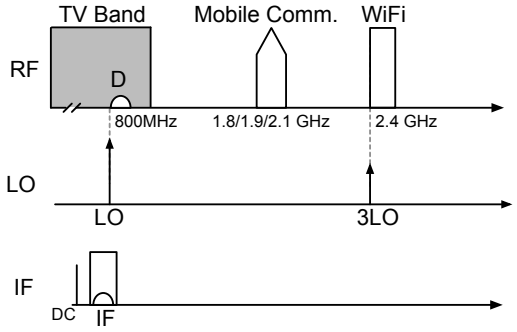
While it is certainly conceivable to accomplish frequency translation through multiplication with quadrature sinusoids, it is typically not done in modern CMOS processes. In the past, analog multipliers in bipolar transistor technology have been built using the trans-linear principle [22]. Such multipliers are noisy and unsuitable for meeting the stringent dynamic range requirement of TV receivers. Secondly, CMOS technology offers good ON-OFF switches. Multiplying by a square wave could simply mean commutating the RF signal between the positive and negative sides of a differential output. This is a function that is easily accomplished through a simple differential pair (active mixer) [23, 24] or a set of 4 hard driven transistors (passive mixer) [25–28]. Since only commutation is involved, the circuit noise in the mixing operation is small compared to analog multipliers.

1.4 The Problem of LO Harmonic Rejection

For a wideband receiver, the harmonics of the square-wave LO, translate unwanted signals around the LO harmonics to the same IF frequency as is shown in Fig. 1.7. ATSC specifies that an interferer 6 channels away can be 57dB stronger than the desired signal while an SNR of 15 dB needs to be maintained [11]. There is no specific test mentioned in [11] when the interferer



(a)



(b)

Figure 1.7: The LO harmonics problem in a wideband receiver.

is around an LO harmonic. But since there is no reason as to why an interferer cannot be present at the LO harmonic, we can deduce a harmonic rejection requirement from the aforementioned test. This tells us that the LO harmonic rejection of 72 dB (= 52 + 15 dB) is needed. While there is no documented specification for analog terrestrial TV, the traditional testing of TVs suggests that a harmonic rejection in excess of 70 dB is also needed here.

1.5 An Overview of Existing Solutions

Earlier solutions to this problem used tuned pre-mixer passive filters implemented using discrete components to remove undesired signals around the significant LO harmonics. However, these solutions are bulky, costly and unsuitable for a low-cost integrated circuit realization. Later, in an effort to solve the LO harmonics problem, up-down dual conversion approaches have been proposed [1,2,29,30]. But these approaches do not offer a true integrated solution as an external SAW filter is required. Besides, this dual conversion approach needs additional mixers and synthesizers, which result in higher power consumption. In the last decade, single conversion receivers based on harmonic rejection mixers (HRMs) have gained increasing popularity[7, 31–33]. While HRMs offer improved performance over conventional square-wave LO mixers, their HR performance is limited to about 30-40 dB [5, 34]. A mixer capable of high HR ratios is needed to relax the requirements on pre-mixer RF filters, which are expensive and bulky. Achievement of high HR ratios in the mixer implies that the pre-mixer RF filters can be built from components available

in a typical CMOS process. High HR ratios in the mixer are thus, crucial for integrated TV tuner solutions. While there have been techniques proposed to achieve improved rejection of the 3^{rd} and 5^{th} harmonics using two-stage mixing [6] and calibration [7, 10], there has not been much work published that achieves improved harmonic rejection for higher order harmonics. For television, the frequencies of the input signals can span over a 17X range (48-860 MHz). Higher order harmonics other than the third or the fifth, fall in-band for several TV channels. Hence, there has been a need for techniques that not only gives better HR ratios for 3^{rd} and 5^{th}, but also for higher order harmonics.

Furthermore, at high LO frequencies, the ratio (N) between the maximum clock frequency available in a receiver to the desired LO frequency can be a small integer (typically less than 10). When N is 4, the un-rejected harmonic is the $(N-1)^{th}$ or the 3^{rd} harmonic. Its rejection is only $20log(N-1)$ or about 10 dB. The un-rejected harmonic can down-convert out-of-band interferers and corrupt the desired signal in the TV band as shown in Fig. 1.7b. Given that there are several out-of-band interferers in the RF spectrum and the trend towards reduced pre-mixer filtering to lower cost, it is desirable that a rejection higher than $20log(N-1)$ dB is available for the $(N-1)^{th}$ harmonic.

1.6 Thesis Statement

Clock-gated harmonic rejection mixers have a reduced sensitivity to mismatches in devices operating at high frequencies and thus, achieve a higher level of harmonic rejection performance.

1.7 Original Contributions

In this thesis, new harmonic rejection mixer architectures are presented to address many issues raised in section 1.5. Following are original contributions.

- A generalized $N-$phase HR mixing technique is presented that has significantly reduced sensitivity to mismatches in devices operating at high frequencies. HR performance for this technique is primarily determined by resistor and capacitor matching at low frequencies. This enables superior HR performance as large resistor areas can be used at low frequencies without any power penalty. This technique has been verified by measured results on silicon fabricated in 110 nm CMOS process.

- For this $N-$phase mixing technique, conversions gains and relative phase for all frequency translations have this reduced sensitivity to mismatches in devices operating at high frequencies. Since the fundamental and the DC component of the effective multiplying waveform have this reduced sensitivity, superior IR and IIP2 performance are realized respectively. A detailed discussion on IR and IIP2 performance benefits for this mixing technique is presented.

- A technique to cancel flicker noise of the transistors in the switching pair in active HR mixers is described.

- The $N-$phase mixing technique rejects the $(N-1)^{th}$ harmonic only by an amount of $20log(N-1)$ dB. A new HR mixing technique is presented

that achieves additional rejection of the previously un-rejected $(N-1)^{th}$ harmonic while preserving the level of rejection for the other harmonics. This technique has been verified by measurements done on an integrated circuit fabricated in 55 nm CMOS process.

- While the published literature has focused only on a 8-phase mixer and the rejection of the third and fifth LO harmonics, this work achieves higher HR performance on higher order harmonics as well. In this dissertation, we present a configurable 16,12,8 and 6 phase HRM rejecting up to the first 14 harmonics using the first technique and a mixer with configurable 14, 12 10 and 8 rejecting up to the first 12 harmonics using the second technique.

- A theoretical analysis of the key performance parameters of gain, noise figure (NF), third-order input-intercept-point (IIP3), IIP2 and HR for the new HR mixer topologies is presented.

1.8 Thesis Organization

The rest of the thesis is organized as follows:

Chapter 2 discusses the existing architectural and circuit level solutions to address the harmonic rejection problem of a wideband receiver. An overview of the HRM concept [4], its generalization to N phases and trade-offs involved in its implementation are discussed in greater detail. The current state-of-the-art is described and merits and demerits of the recent advances are identified.

Chapter 3 elaborates on the technique presented in [35,36], which overcomes a key limitation caused by phase errors in the current state-of-the-art in achieving a higher level of HR performance. The design of the mixer using this technique with a programable number of 16, 12, 8 or 6 mixer phases and fabricated in 110 nm CMOS process is discussed in greater detail. The measured harmonic rejection ratio is in excess of 52 dB for all rejected harmonics, while also canceling flicker noise and achieving a higher IIP2 performance. The key performance parameters for the mixer including gain, noise figure, IIP2, IIP3 and HR ratios are also discussed.

Chapter 4 elaborates on the enhanced technique presented in [36, 37], to achieve a higher level of rejection for the $(N-1)^{th}$ LO harmonic without compromising the level of rejection for other harmonics. The design of the mixer using this technique with a programmable number of 14, 12, 10 or 8 mixer phases and fabricated in 55 nm CMOS process is presented. This mixer achieves an improvement of 29 dB for the $(N-1)^{th}$ LO harmonic while achieving 52 dB of rejection for the 3^{rd} harmonic. A theoretical analysis of the IIP2 performance and flicker noise cancelation is also presented.

Chapter 5 draws conclusions, summarizes the main contributions of this work and suggests some future research directions.

Chapter 2

Current Solutions

2.1 Evolution of Architectures in Wideband Receivers

This section gives an overview of the conventional architectures that have been used to solve the LO harmonic rejection problem.

2.1.1 Discrete RF filter Based Solutions

This was one of the earliest architectures used in television. It is also called an MOPLL solution (MOPLL standing for Mixer, Oscillator and PLL), since the integrated circuit used in this approach incorporated only these functions. The rest of the components (RF filter, low noise amplifier and surface acoustic wave (SAW) filter) were implemented using discrete components. In this solution, amplified RF signals are filtered using an off-chip discrete com-

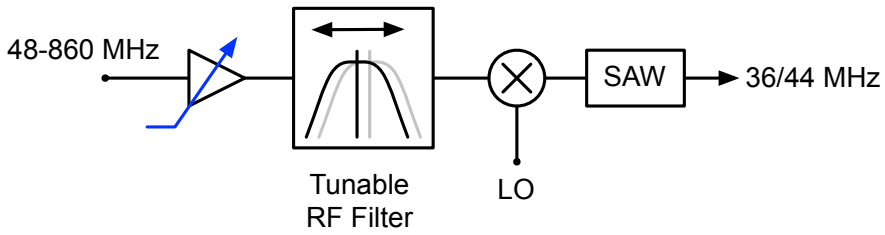


Figure 2.1: Discrete RF Filter Based Solution

Figure 2.2: An MOPLL Board

ponent filter. The filter is tunable across a particular terrestrial TV band. A three-band solution is typically used to cover the terrestrial TV bands of VHF-L (54-88 MHz), VHF-H (174-216 MHz) and UHF (470-806 MHz). The tunable filter is typically realized either using a cascade of a second-order LC bandpass filter and a fourth-order filter using coupled resonators. The mixer used in this approach is non-quadrature square-wave mixer. It has poor third harmonic rejection (˜ 10 dB) and also suffers from the image problem [21]. Hence, a high-order pre-mixer filter (up to 6) is necessary to remove interferers around the LO harmonics. The image problem is addressed by having a tunable notch in the tracking filter at an offset of twice the intermediate frequency from the desired channel. The IF frequency is 36 or 44 MHz and channel selection is accomplished through an external SAW filter at the IF frequency. The tuning of the RF filter is accomplished through high voltage varactors (typically 30V). The tracking filter is bulky, complex, expensive and is not amenable to an integrated circuit realization.

A board showing the MOPLL is depicted in Fig. 2.2. As can be seen,

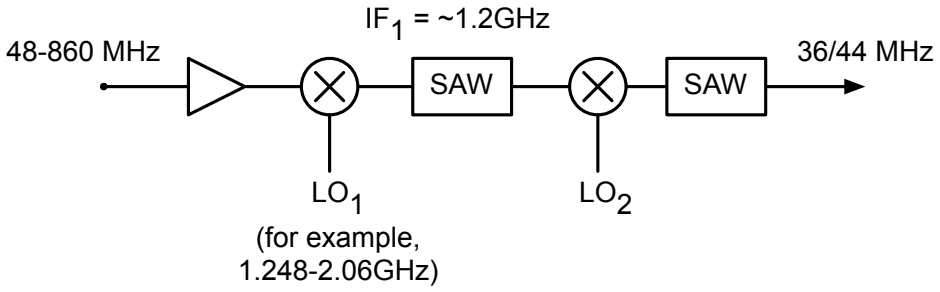


Figure 2.3: Up-Down Conversion Based Architecture [2]

several discrete coils (inductors) are used in the realization of tracking filters for multiple bands. Hand tuning of the coils is used to adjust the values of the inductors and center the band-pass filters. More recently, a simplified tracking filter in integrated within the tuner package (but not in the same tuner silicon die) in [38]. Other more recent implementations can be found in [39, 40].

2.1.2 Up-Down Conversion Architecture

This architecture [2,41,42] (shown in Fig. 2.3) solves the LO harmonics problems by up-converting the desired RF signal to a high IF frequency, IF_1. While [2] uses an IF_1 1.12 GHz, [41, 42] use an IF_1 of 1.22 GHz. The up-converted signal is filtered through a SAW filter centered at IF_1. Since the LO signal used in the first up-conversion (LO_1) is at a high frequency (e.g. 1.2-2.1 GHz), the harmonics of LO_1 are also at a high frequency. For example, the 3^{rd} harmonic of LO_1 ranges can range from 3.6-6 GHz. RF signals frequency translated by the third harmonic of LO_1 that can appear at the output of the first SAW filter, will have to lie at $3LO_1 \pm IF_1$ GHz. This is out of the desired

TV band. Square wave mixers with third harmonic rejection of only 10 dB are used for up/down-conversion. The output of the first SAW is subsequently down-converted by a second LO signal (LO_2) to a standard IF of 36/44 MHz. There are no interferers present at the output of the first SAW filter around the harmonics of LO_2. So the harmonics of LO_2 do not cause spurious down-conversions. There have been several variations in the implementation of this architecture. In [29], the second down-conversion is to a zero IF. [30] also uses an IF_1 of 1.22 GHz while targeting OpenCable applications [19], but uses quadrature mixing for the second down-conversion. An IF_1 of 1.892 GHz is used in [43] to minimize the tuning range on LO_1 but it also uses quadrature mixing for the second down-conversion. In [16], low-IF down-conversion is used for the second mixing operation while suppressing the image digitally using a LMS signal de-correlation algorithm. [1] applies this architecture for meeting the requirements of analog and digital multi-standard television.

Though this architecture solves the LO harmonics problem, its implementation is costly as it typically needs additional filters. Higher power is consumed in the generation of the two LO signals. Also, the phase locked loops used to generate the two LO signals take additional die area. This results in high cost as well making this architecture unfavorable for a low-cost integrated TV tuner.

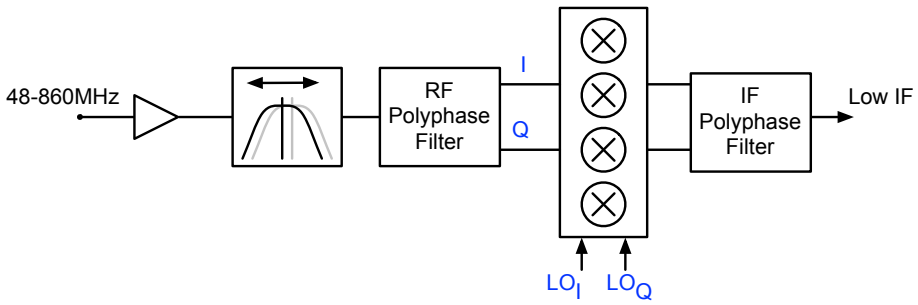


Figure 2.4: Double Quadrature Downconversion [3]

2.1.3 Double-Quadrature Down-conversion

This approach [3, 38] (Fig. 2.4) uses the fact that for a quadrature square-wave down-conversion mixer, the LO spectrum has components only at $+LO$, $-3LO$, $+5LO$ and so on. There is no LO spectral energy at $+3LO$ and $-5LO$. An RF poly-phase filter [44] is used after low-noise amplification and band-pass filtering to reject close interferers. The poly-phase filter's output is complex and in the complex frequency spectrum, RF signal at $+3LO$ is rejected while preserving the signal at $-3LO$. Since the LO spectrum does not have a component at $+3LO$, 3^{rd} harmonic rejection is achieved. However, this technique requires four real mixers with quadrature RF and quadrature LO signals as its inputs. Ideally the effective LO spectrum has components only at the 5^{th},9^{th},11^{th}... harmonics. But gain and phase errors in the quadrature RF and LO signals can affect the 3^{rd} harmonic rejection.

While this approach enables a higher level of third harmonic rejection and relaxes the requirements on the pre-mixer filter, the 5^{th} harmonic is not rejected, for which a tunable RF filter is needed as shown in Fig. 2.4. Due to

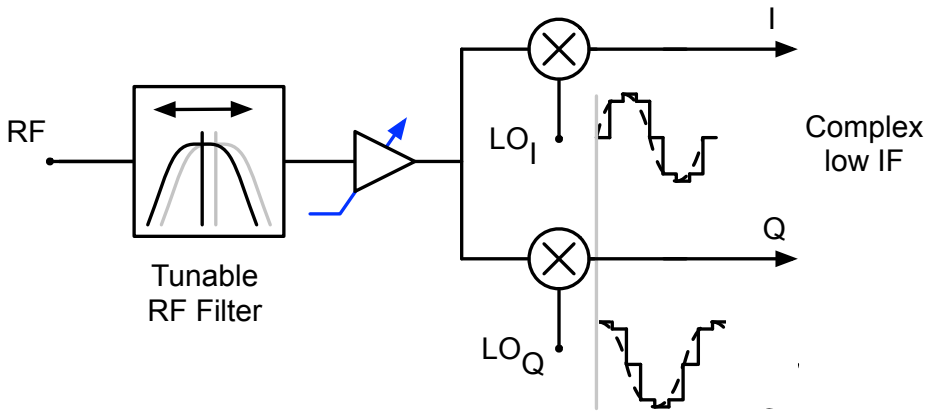


Figure 2.5: HRM with pre-Mixer RF filters

the relaxed pre-mixer filtering requirements, this architecture is more suitable for a low-cost integrated circuit realization than the earlier solutions.

2.1.4 HRM with pre-Mixer Filters

In this approach shown in Fig. 2.5, the filtered and amplified RF signal is multiplied with a quadrature LO signal. LO_I and LO_Q are stair-case approximations to a sinusoid. Thus, this LO has less harmonic content than a square-wave. For an N step approximation to a sine wave, harmonics till the $(N-1)^{th}$ are rejected. In a practical implementation however, non-idealities cause the rejection to be finite. For conventional implementations of this mixing operation, the 3^{rd} harmonic rejection is in the 30-40 dB range [5, 34]. Analog and Digital TV standards demand an effective LO harmonic rejection in excess of 70 dB. Hence, this approach still needs a pre-mixer filter to partially remove interferers around the LO harmonics. But compared to earlier

approaches, the pre-mixer filter requirements are more relaxed. Variant of this approach for the special case of $N = 8$ is used in [31, 45].

2.2 Trend in Architectural Evolution

At this stage, it is useful to evaluate the trends in the architectural evolution of receivers for the TV. Broadly speaking, the architectures described in the earlier section can be categorized into two categories: 1) Dual Conversion Approaches and 2) Single Conversion Architectures. Dual conversion involves two mixing operations. The Up-Down Architecture described in section 2.1.2 comes under this category. Single conversion architectures use only one mixing operation. The desired RF channel is down-converted to a standard IF (36/44 MHz), low-IF or DC in a single step. Architectures described in sections 2.1.1, 2.1.4, 2.1.3 fall into this category. The up-down architecture solves the LO harmonic rejection problem but is costly and consumes higher power than the single conversion approaches. While the dual conversion architecture was popular in the early parts of last decade (years 2000-2005) [2, 29, 30, 41–43], in more recent years (2007-present) the single conversion architectures have gained increased traction [5–7, 31, 35, 37, 45].

Examining the single conversion approaches reveals an interesting trend (shown in Fig. 2.6). The tunable RF filter architecture uses a mixer with poor harmonic rejection (˜10 dB) and needs costly high-order pre-mixer filter. Double quadrature mixing improves the 3^{rd} harmonic rejection and relaxes the filtering requirements while lowering the cost. A 16-phase HRM [35, 37] pre-

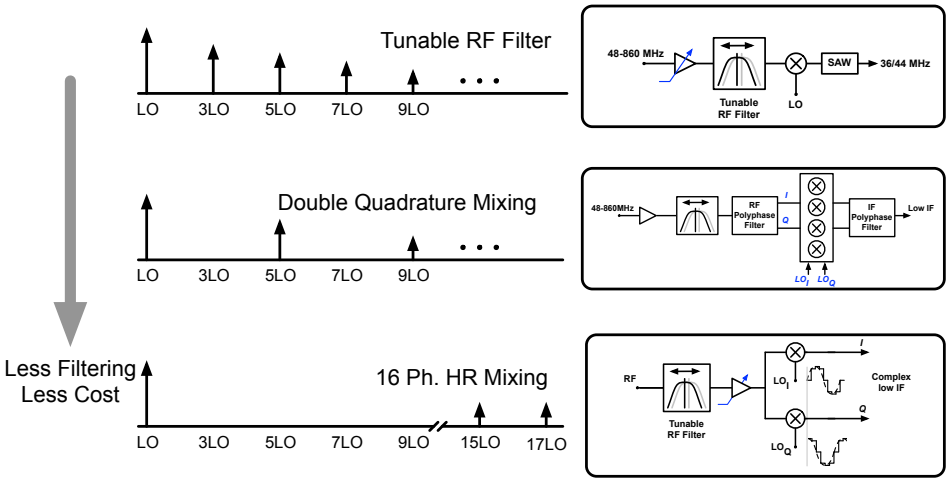


Figure 2.6: Trend in Single Conversion Architecture Evolution.

sented in this dissertation further drives the filtering requirements down while lowering the cost of the overall solution even further. This is consistent with the drive in the semiconductor industry to reduce costs. This also underscores the importance of a HRM that is capable of a high level of rejection for all relevant harmonics in a wideband receiver.

2.3 Harmonic Rejection Mixing

2.3.1 Concept

The key idea in HRM [4] consists of approximating the sine wave by weighting and adding time-shifted square-waves in order to cancel their third and fifth harmonic components as explained in Fig. 2.7a. Since the phase shift between the fundamental components of $LO1$ and $LO2$ as well as $LO2$ and $LO3$ is 45^o, their third harmonics differ by three times as much (135^o) and

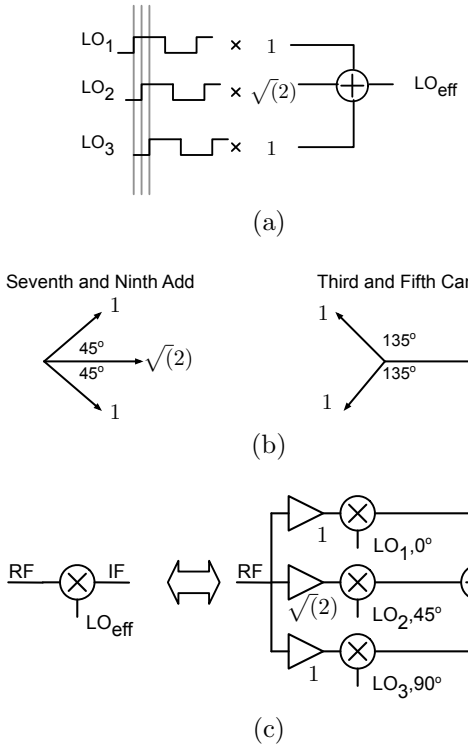


Figure 2.7: HRM Concept. (a) Time domain weighting and addition of square waves. (b) Harmonics of square wave in phasor notation. (c) Implementation.

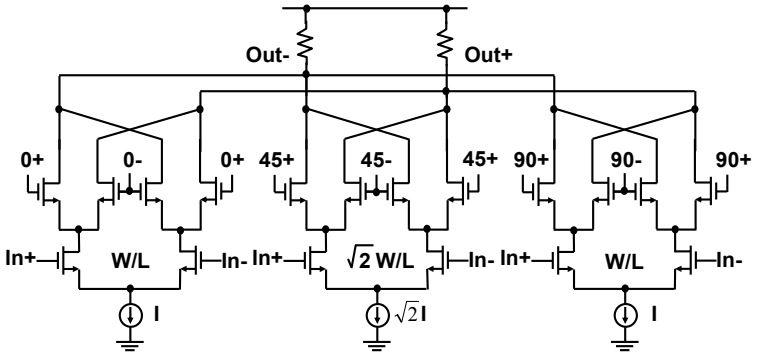


Figure 2.8: Circuit implementation of [4]

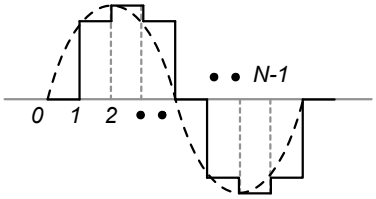


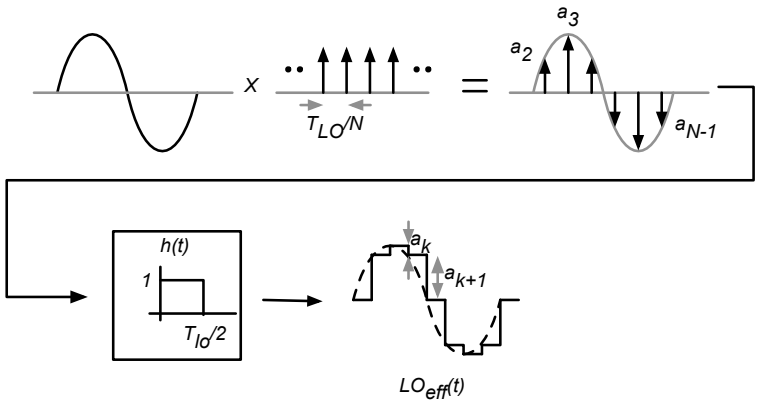
Figure 2.9: An N point approximation to a sinusoid.

their fifth harmonics by five times (225^o). This results in their cancellation as shown. However, their seventh and ninth harmonics do not cancel.

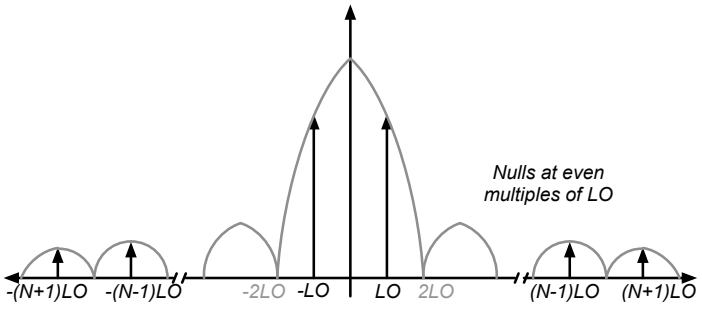
A circuit implementation of this HRM concept is shown in Fig. 2.8.

2.3.2 Generalization of HRM Concept to N phases

The HRM concept can be easily extended to reject more LO harmonics. Referring to the LO_{eff} waveform in Fig. 2.9, it is intuitive to expect that a better approximation to a sine wave with more sample points, results in cancellation of more harmonics. A possible N-point approximation to the sine wave is shown in Fig. 2.9.

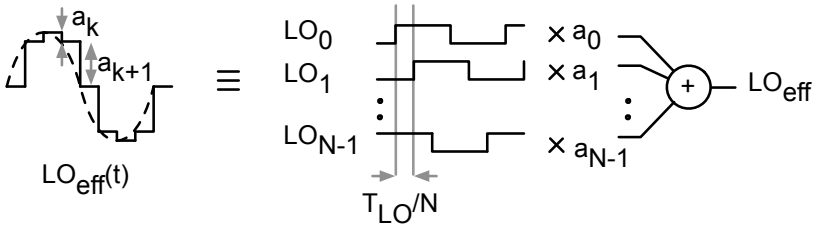


(a)

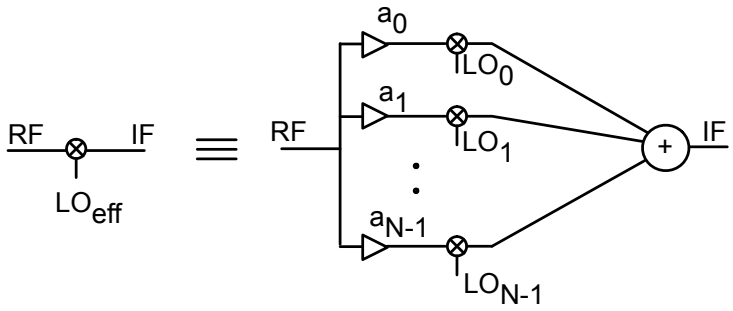


(b)

Figure 2.10: Constructing LO_{eff} (a) in time domain. (b) in frequency domain.



(a)



(b)

Figure 2.11: Generalized N-phase HRM.

Mathematically, this can be thought of as a sine wave being ideally sampled at N times its frequency and the output passed through a filter whose impulse response is a rectangular pulse, or a zero-order-hold (ZOH), as shown in Fig. 2.10a.

In the frequency domain, the resulting spectrum is series of impulses at $(k \cdot N \pm 1) \cdot LO$ shaped by the sinc function with zeros at $2k \cdot LO$ (k being any integer), as shown in the Fig. 2.10b.

Equivalently, LO_{eff} can be expressed as a weighted sum of time-shifted square waves as shown in Fig. 2.11a. Since mixing is simply multiplication of

RF and LO, we write the product IF as

$$IF(t) = RF(t) \cdot LO_{eff}(t) \tag{2.1}$$

$$IF(t) = RF(t) \cdot \left(\sum_{k=0}^{N-1} LO_k(t) \cdot a_k \right) \tag{2.2}$$

$$IF(t) = \sum_{k=0}^{N-1} \left(a_k \cdot RF(t) \right) LO_k(t) \tag{2.3}$$

An equivalent block diagram of the generalized HRM is shown in Fig. 2.11b.

A circuit representation of the concept is shown in Fig. 2.12. RF transconductors are weighted in proportion to the samples of a sine wave ($a_k = sin(\frac{2\pi k}{N})$). RF transconductor currents flow through differential-pairs switched by time-shifted square waves. The time shift between two adjacent LO waveforms is proportional to $\frac{2\pi}{N}$. Note that since the switching pairs steer RF current to either the positive or negative IF output, the number of RF transconductor slices is only $\frac{N}{2}$. (The other half of the sine wave in the LO_{eff} waveform is generated through the negative half cycle of the differential LO_k waveform.) While a single balanced implementation is shown in Fig. 2.12 this concept can be easily extended to a double balanced realization as well.

2.3.3 Gain and Noise Performance

Since the RF transconductor currents are multiplied by time shifted LO waveforms, they undergo a phase shift prior to summation at the IF output.

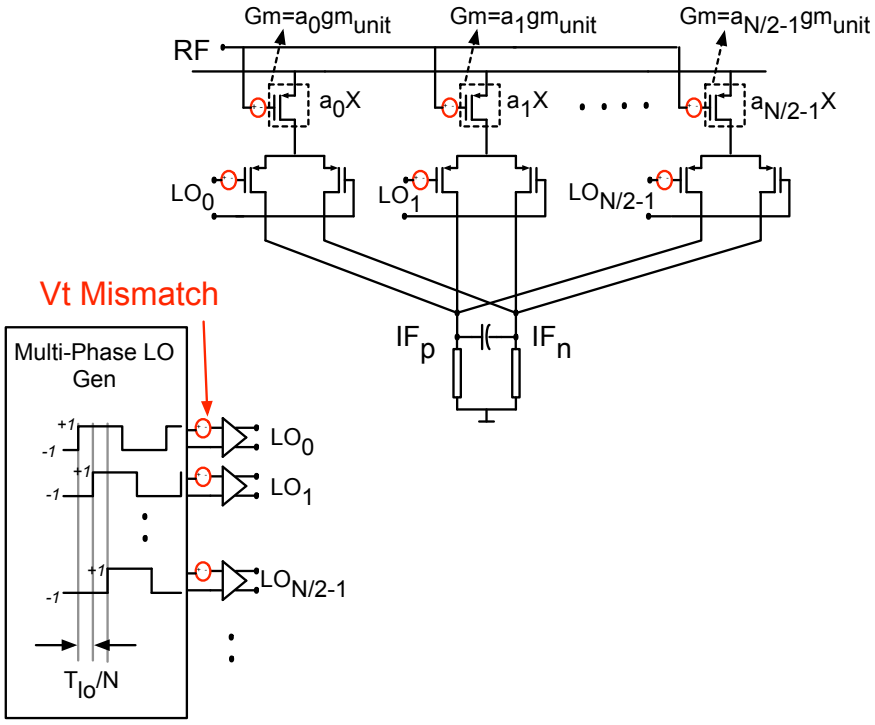


Figure 2.12: Circuit Implementation of N-phase HRM.

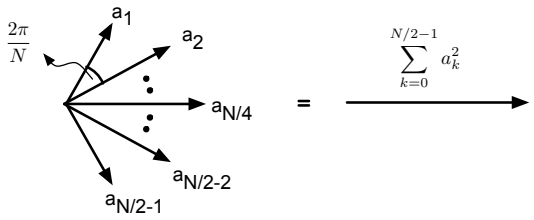


Figure 2.13: Loss of Gain in HRM

This phase shift for the harmonic components is necessary for HR, but for the fundamental this results in a loss of Gain. Figure 2.13 shows the signals at IF from different RF transconductor legs in phasor notation. For ease of illustration, it is assumed that N is a multiple of 4 and $a_k = sin(\frac{2\pi k}{N})$. The resultant of these phasors can be easily shown to be the sum of squares of the magnitudes of the individual phasors (Figure 2.13). As the magnitude of each a_k is lesser than 1, the magnitude of the resultant is smaller than $a_1 + a_2 + \ldots a_{N/2-1}$. Thus, compared to the case when all the transconductor legs are all switching at the same LO phase, there is a loss of gain (L).

$$L = \frac{a_1^2 + a_2^2 + \ldots a_{N/2-1}^2}{a_1 + a_2 + \ldots a_{N/2-1}} \tag{2.4}$$

From a noise perspective, note that the total output thermal noise remains the same, irrespective of the number of LO phases (or N) if the total transconductor current is kept the same. This is because each switching pair only switches the polarity of the white noise current of the transconductor. (Effectively multiplying the noise current by +1 or a -1 as it steers the current to IF_p or IF_n respectively). Since switching the polarity of a white noise waveform in time domain every half period of LO cannot change the power

Mixing Scheme	Gain	Input Referred Thermal Noise
non-HR	1.00X	1.00X
N=8	0.83X	1.20X
N=12	0.80X	1.25X
N=16	0.79X	1.26X

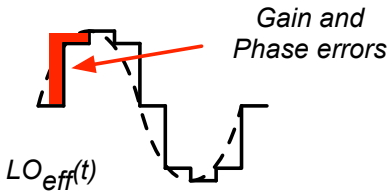
Table 2.1: Gain and Noise as a function of N

spectrum of the noise current, the PSD of the output noise is independent of the phase of LO and only proportional to the transconductor current. Since the thermal noise current in each transconductor, is uncorrelated with others, the total output noise remains the same irrespective of N.

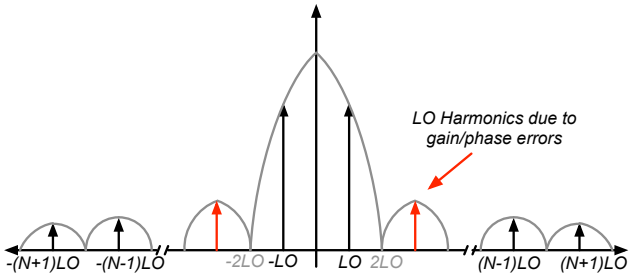
Table 2.1 shows the Gain and input referred noise for different N compared with a non-HR scheme. As can the seen, this HR mixing technique trades-off Gain and Noise Figure for the same total current in order to achieve harmonic rejection.

2.3.4 Trade-off in Harmonic Rejection

Referring to Figure 2.12, in the presence of mismatches the transconductor currents are no longer in exact proportion to the sine wave samples a_k. Further the switching instant of currents in the differential switching pairs is affected by the mismatches in the multi-phase LO generation circuitry. This results in gain and phase errors in the LO_{eff} waveform as shown in Figure 2.14a and 2.14b. In the frequency domain, these gain/phase errors manifest themselves as LO harmonics, thus degrading the harmonic rejection performance of the mixer.



(a) LOeff(t) with Gain/Phase errors



(b) Spectrum of LOeff with Gain/Phase errors

Figure 2.14: Impact of gain/phase errors

The only way to achieve higher harmonic rejection in this mixer, is to reduce the standard deviation (σ_{Vt}) of the mismatches that cause the gain/phase errors. But since $\sigma = \frac{A_{Vt,\beta}}{\sqrt{WL}}$, this entails a higher device area. For the RF transconductors, this results larger input capacitance and lowering of the RF bandwidth between the LNA and the mixer. In order to reduce the phase errors in multi-phase LO generation, large W/L ratios are needed in the devices that generate the multi-phase LO. The increased capacitance results in higher dynamic power dissipation.

Thus, a key limitation of this topology is that higher HR cannot be achieved without burning power or causing a reduction in the RF bandwidth.

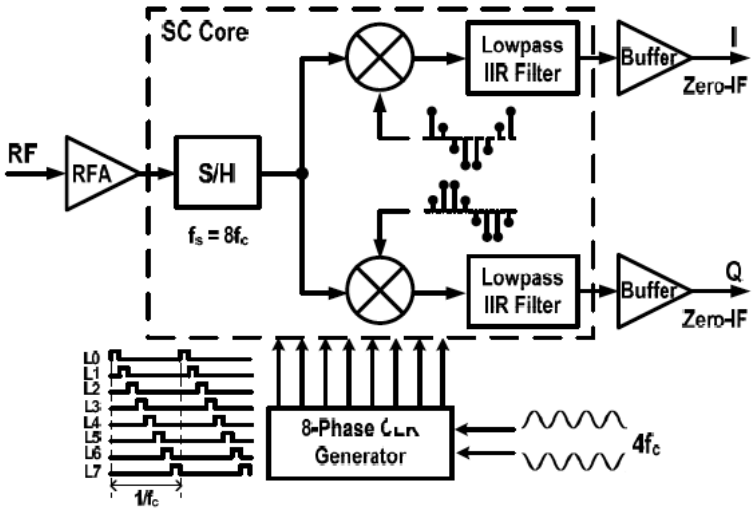


Figure 2.15: Architecture of HR Sampling Downconverter [5]

2.4 Recent Advances in HRMs

2.4.1 Discrete-Time HR Mixing

In order to benefit from the short transistor dimensions and superior integration offered by advances in CMOS technology, discrete-time samplers have been proposed for frequency translation in receivers [46, 47]. These samplers allow for more discrete-time and digital signal processing. However, when applied to wideband receivers like television or software-defined radios, these samplers also suffer from folding of interferers around harmonics of the sampling clock. [5] proposes a discrete-time HR mixing architecture shown in Fig. 2.15 and discusses its suitability for software-defined radios in [48]. This architecture is intended for DVB-H receivers operating in the 470 to 862 MHz frequency range and for cognitive radio applications in 200 to 900 MHz band where 3^{rd} and 5^{th} harmonic rejection is a concern. In this architecture,

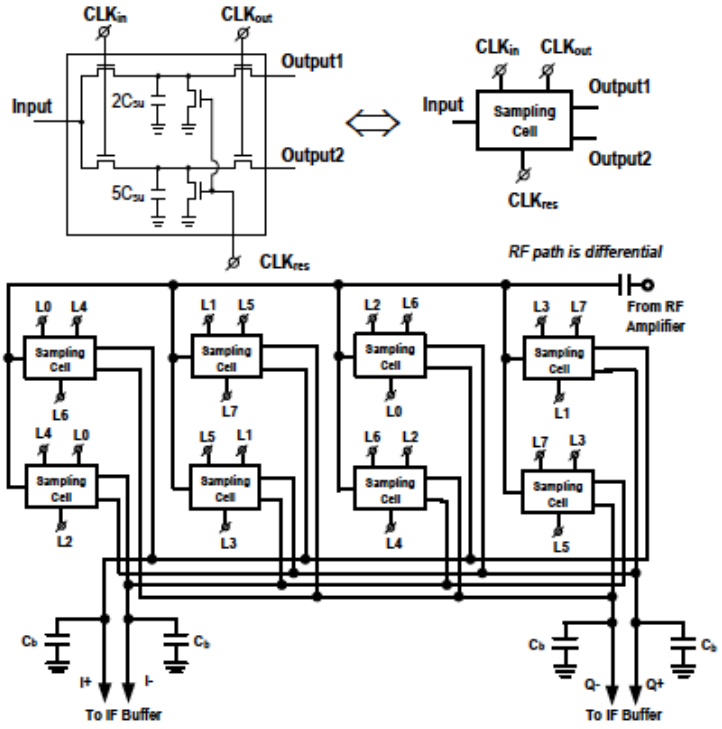


Figure 2.16: Switched capacitor core used in [5]

the amplified RF signal drives a passive switched-capacitor core consisting of three stages. The first stage is an over-sampler, with the sampling frequency being 8 times the carrier frequency. The second stage consists of discrete-time quadrature mixers. The third stage is a low-pass IR filter.

The implementation of the switched capacitor core is shown in Fig. 2.16. A unit capacitor used in the ratio of 2:5 implements the sine weights. Two capacitors, $2C$ and $5C$, enable the implementation of the $5 : 7 : 5$ approximation, where C is the unit capacitor. The discrete-time mixing function is implemented via a systematic combination of the output switches, to trans-

fer charges from the sampling capacitors to buffer capacitors. In addition to weighting, the charge sharing between the sampling and buffer capacitors also implements a low-pass filter.

This technique also suffers from problems similar to that of a conventional HRM. The clock timing mismatches are significant and degrade the HR performance. The actual values of sine weights differ from ideal due to layout parasitics and mismatches. This causes gain errors. While being more suitable for digital intensive receivers in finer geometry technologies, this technique only achieves 3^{rd} and 5^{th} harmonic rejection between 32-41 dB.

2.4.2 2-Stage HR Mixing

Ru et al. describe a technique to substantially reduce gain errors in HR mixers in [6] . The block diagram is shown in Fig. 2.17. The sine-weighting in this technique happens in two stages. In the first stage, RF transconductors are weighted in the ratio of $2 : 3 : 2$ (approximating the values of a sine wave at 45, 90 and 135 degree angles). The mixer multiplies the weighted-currents of RF transconductor with 1/8 duty cycle LO waveforms to generate multi-phase IF outputs. These multi-phase outputs are further weighted by approximations of a sinusoid $(5 : 7 : 5)$ and summed to generate the final quadrature output.

The output of TIA1 has 8 IF-outputs with equidistant phases, i.e. 0 to 315 with 45 step. Weighting and summing the three adjacent phase outputs of the first stage via the second-stage weighting factors of $5 : 7 : 5$ results in a

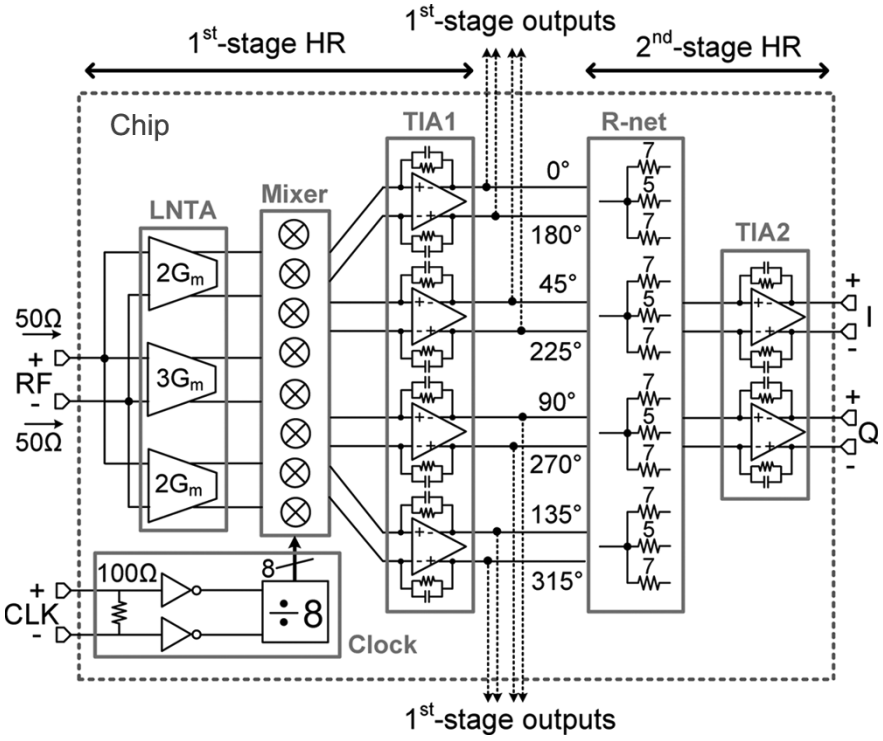


Figure 2.17: 2-Stage HR Mixing from [6]

$$
\begin{array}{r}
[\,2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3} \quad -2 \quad 0] \cdot 5 \\
+\,[\,0 \quad 2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3} \quad -2] \cdot 7 \\
+\,[-2 \quad 0 \quad 2 \quad \mathbf{3} \quad 2 \quad 0 \quad -2 \quad \mathbf{-3}] \cdot 5 \\
\hline
[\,0 \;\; 29 \;\; 41 \;\; 29 \;\; 0 \;\; -29 \;\; -41 \;\; -29]
\end{array}
$$

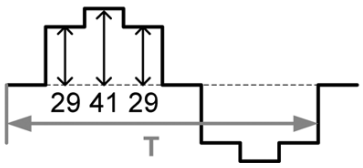


Figure 2.18: 2-Stage HR Mixing from [6]

better approximation to a sine wave of 29: 41: 29, as shown in Fig. 2.18. The 3rd HR ratio for this is in excess of 77 dB. Thus, despite starting from poor approximations to sine weights in the first and second stages, this technique achieves a very precise sine wave. Another way of looking at this is that the gain errors in the implementation of sine-weights in the first and second stages cause a much smaller degradation in the HR ratios. In the absence of phase errors in the multi-phase LO, the HR performance for this technique is determined by the product of gain errors in the first and second stages, which is smaller than the gain error in either of the stages.

The phase errors, however, do not benefit from the 2-stage mixing. The phase error in the multi-phase LO generation directly impacts the HR performance similar to a conventional HRM. This ultimately limits the HR performance achievable using this technique. In order to reduce the phase error in multi-phase LO generation large W/L ratios are necessary in the flip-flops and drivers generating the multi-phase clock. Since multi-phase LO generation happens at a high clock frequency, a substantial dynamic current is consumed. Thus, this technique too suffers from the trade-offs similar to a conventional HRM with respect to phase errors.

2.4.3 Calibration using Analog knobs

Greenberg et al. use programmability in the analog section of the HRM to finely adjust the gain/phase of the multi-phase LO in [7]. However, this approach requires a calibration signal to find the gain/phase errors in a

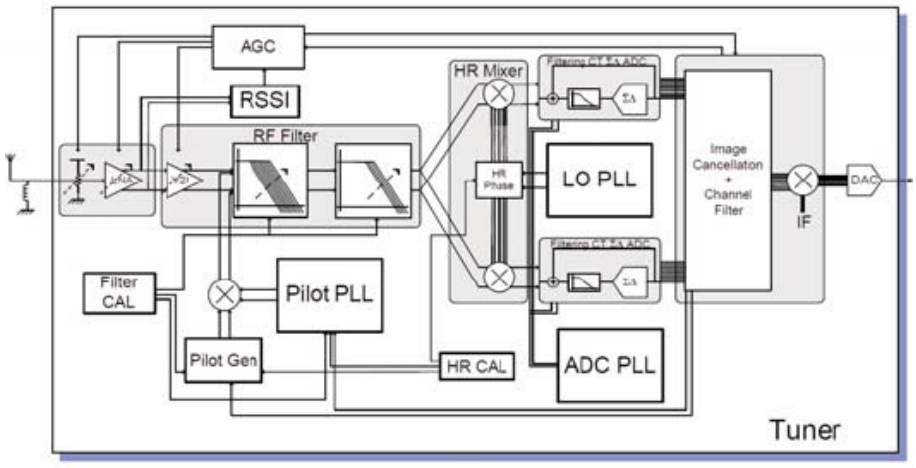


Figure 2.19: Receiver Architecture used in [7]

particular chip. The architecture of the receiver used in [7] is shown in Fig. 2.19. An auxiliary PLL is used to generate a pilot tone that is injected prior to the mixer in the signal chain. Phase of the multi-phase LO is adjusted in the analog domain to cancel the phase errors due to device mismatches. The duty-cycle of the LO is also adjusted for improved rejection of even harmonics. [49] presented another such calibration based solution.

In addition to the hardware complexity, a key concern with such a calibration scheme is the drift of gain/phase errors with temperature. For a television receiver, the reception is continuous in time. In other words, the receiver can be processing the TV signal continuously for several hours. During this time, the temperature of the receiver can change significantly. Also, pilot signal cannot be injected in the meantime, as it can cause interference to the TV signal being watched. Hence, it is important that the drift in gain/phase

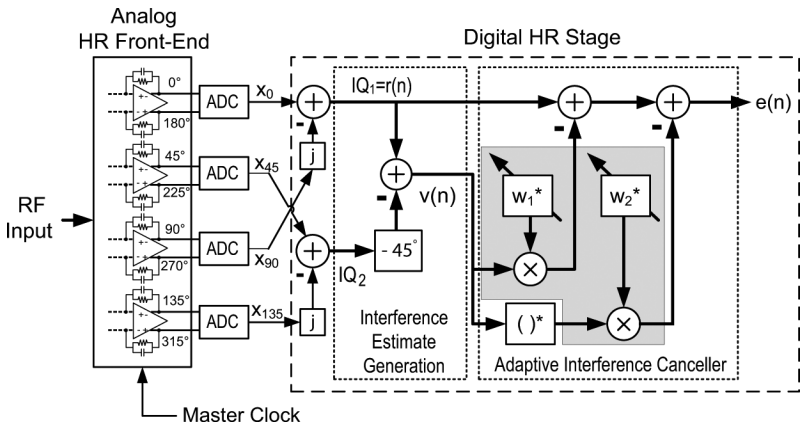


Figure 2.20: Adaptive Interference Cancellation from [8–10]

errors be small enough through out the temperature range, which in itself is a significant challenge.

2.4.4 Adaptive Interference Cancellation

Adaptive algorithms in the digital domain to achieve better HR performance are discussed in [8, 9]. In [10], the concepts of adaptive interference cancellation are applied for improved HR performance in a 400-to-900 MHz software-defined radio receiver. The block diagram of the implementation presented in [10] is shown in Fig. 2.20.

The analog front-end used is identical to the first stage of the two stage HR mixing shown in Fig. 2.17. It produces four differential signals, which are converted into the digital domain using four A/D converters. The HR for the analog down-conversion mixer is in 30-40 dB range. The gain/phase errors in the down-conversion HRM cause the desired signal in $r(n)$ to be corrupted by

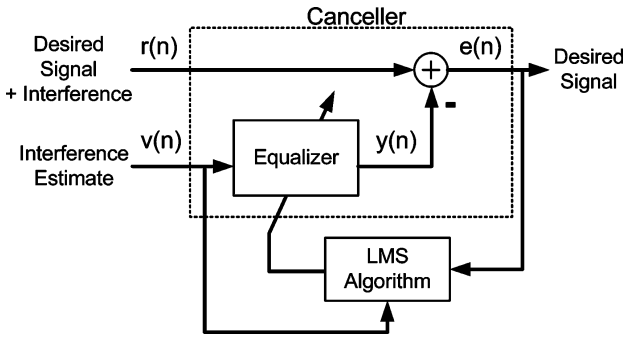


Figure 2.21: Concept of Adaptive Interference Cancellation from [8–10]

interferer from around the LO harmonic. The adaptive interference canceler concept shown in Fig. 2.21, subtracts an estimate of the interferer $v(n)$, from $r(n)$. The equalizer consists of two single-tap FIR filters, which are formed by complex coefficients, w_1 and w_2 and the multipliers shown in Fig. 2.20. The coefficients are adapted using the LMS algorithm. This technique achieves a rejection of 80 dB [10], for a single LO harmonic (either the third or the fifth but not both) by correcting both amplitude and phase of that harmonic image. It does not achieve additional rejection for the other harmonic image. The rejection for the other harmonic is determined by gain/phase errors in the analog portion of the HRM, which is in the 30-40 dB range. Even harmonic rejection is also not improved through the digital ACI.

Application of this technique to a wideband system like television is at least difficult for the following reasons. Firstly, the input frequency range for television spans from 48-860 MHz. The ratio between the maximum to the minimum frequency is 17X. This implies that harmonics other than 3^{rd}

and 5^{th} can fall in-band for several TV channels. In other words, better HR performance is needed not just for the 3^{rd} or 5^{th} harmonics but for higher order harmonics as well. Secondly, simultaneous presence of interferers around both 3^{rd} and 5^{th} harmonics is very much a possibility for systems like Cable television where the input frequency range from 48-860 MHz is continuously loaded with 130 TV channels. In order to achieve better HR performance simultaneously for all harmonics (up to 17^{th}), this technique of digital ACI will require a much more complex algorithm to subtract all the interferers from the corrupted desired signal. Secondly, a large number of A/D converters will be needed to digitize all the relevant multi-phase outputs of the mixer. This will cause a significant increase in power dissipation of the receiver making this approach unattractive.

2.5 Conclusions

In this chapter, we presented the evolution in the architecture of wide-band receiver to solve the LO HR problem. We identified the trend in the architecture evolution to be towards lowering the total cost of receiver. We discussed the importance of a HRM that achieves a higher level of harmonic rejection in lowering the cost. We described the HRM concept and examined the trade-offs involved in achieving a higher level of HR. Finally, we described the recent advances in the state-of-the-art and discussed the short-comings of existing solutions.

Chapter 3

N-Phase HRM with NLO Clock

3.1 Concept

The concept used in this technique is shown in Fig. 3.1. Multi-phase IF outputs are generated by multiplying the RF signal with a clock, called master LO, having N times the desired LO frequency and rotating the product to obtain N IF outputs through the rotational switch S. The switch S transitions from one IF output to the next only when there is no signal through it. This reduces the sensitivity to the noise introduced by the switch and the phase errors caused by multiplication. The low frequency IF signals after down-conversion at $IF_0 - IF_{N-1}$, are then scaled by weights proportional to sine wave samples and summed to produce the final IF_{out}, where all LO harmonics except $mN \pm 1$ are rejected (m being any integer).

3.2 RF Section Implementation and Operation

In the multi-phase mixer shown in Fig. 3.2, RF transconductor current is cyclically rotated to the N IF ports, through master LO transistors, $MP - MN$, and rotational switches, $RP_0 - RP_{N-1}$ and $RN_0 - RN_{N-1}$. Only a single balanced mixer is shown here for clarity. The current flows into any one of

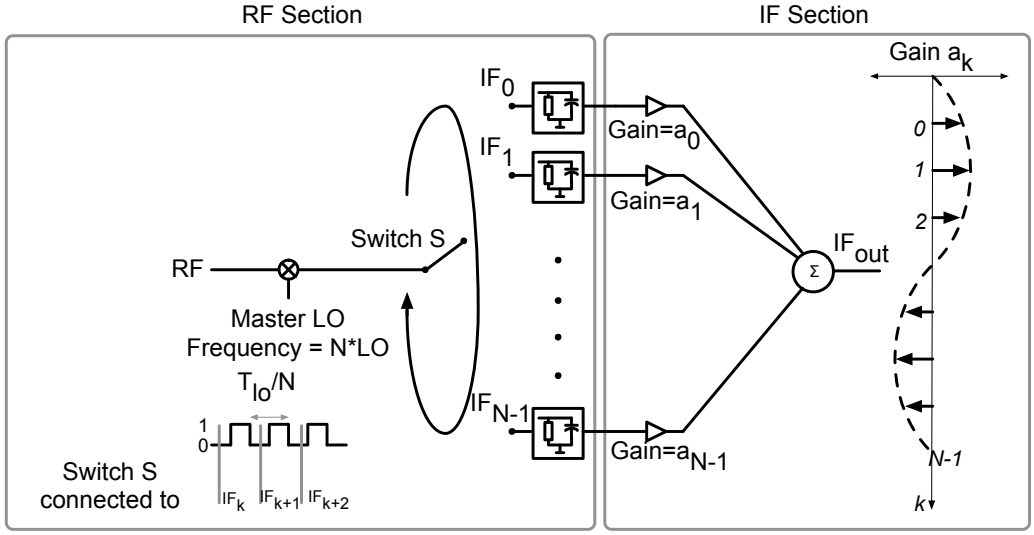


Figure 3.1: Concept of rotational HRM.

the N IF ports for $(1/N)^{th}$ of the time period of LO. During the positive and negative phases of NLO, RF transconductor current flows through the paths via $MP-RP_k$ and $MN-RN_k$ to an IF_k, respectively. Rotation of RF current to IF_{k+1}, continues in the next cycle of NLO through RP_{k+1} and RN_{k+1}. The transitions at the gates of rotational switches happen only when they carry no instantaneous current. An N-stage shift register having master-slave flip-flops is used to generate the rotational pulses. Gating signals for $RP_0 - RP_{N-1}$ and $RN_0 - RN_{N-1}$ are triggered off of the falling edges of NLO_p and NLO_n respectively as shown in Fig. 3.3.

The operation of this rotational arrangement is equivalent to multiplying the RF signal by $1/N$ duty cycle rectangular waveforms that are time-shifted as shown in Fig. 3.4. Shunt capacitors (C) in parallel with load resistors

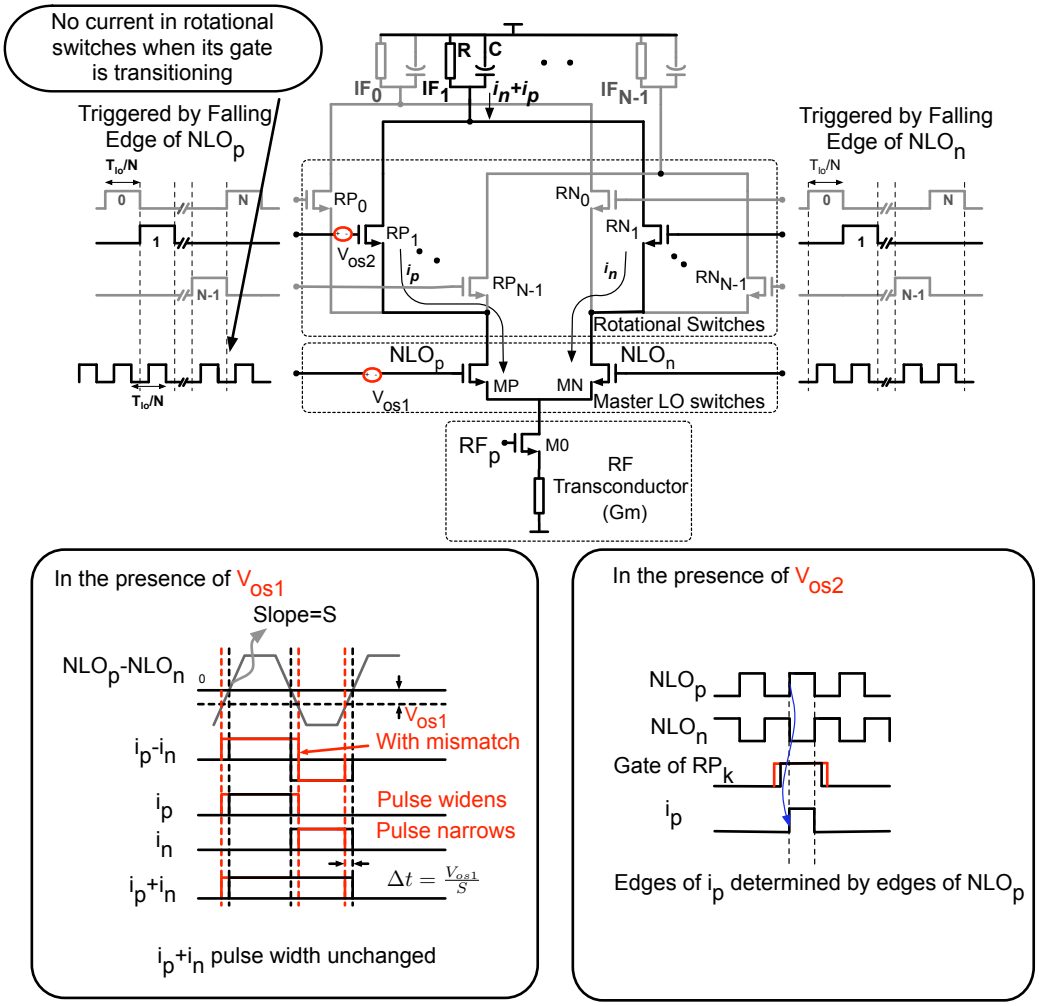


Figure 3.2: Circuit of RF Section.

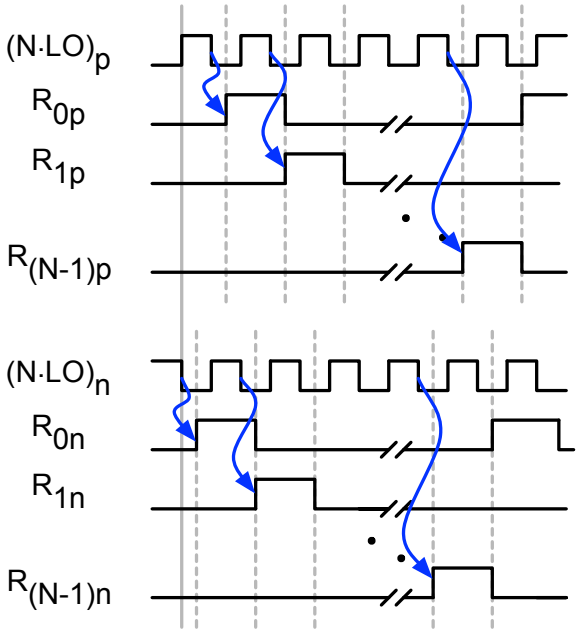


Figure 3.3: Multi-phase LO generation.

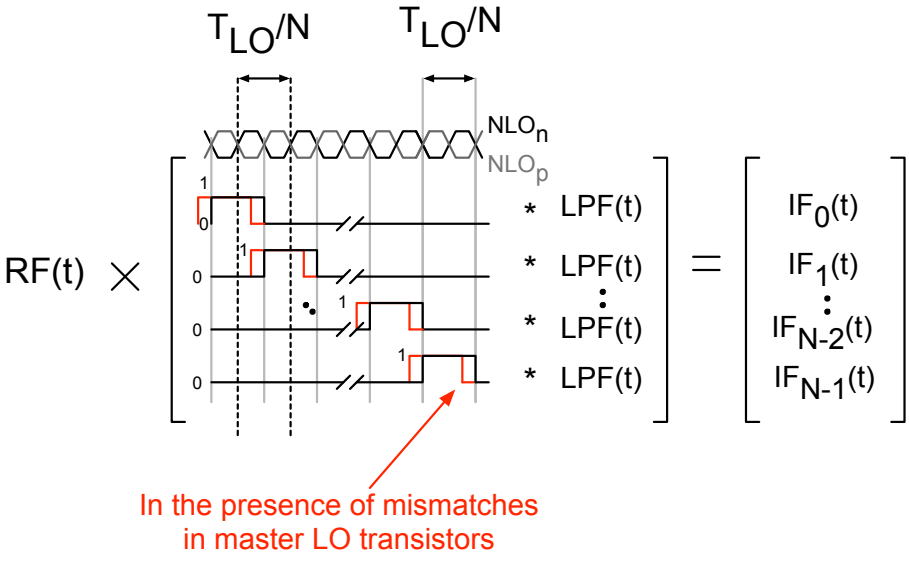


Figure 3.4: RF Section functionality.

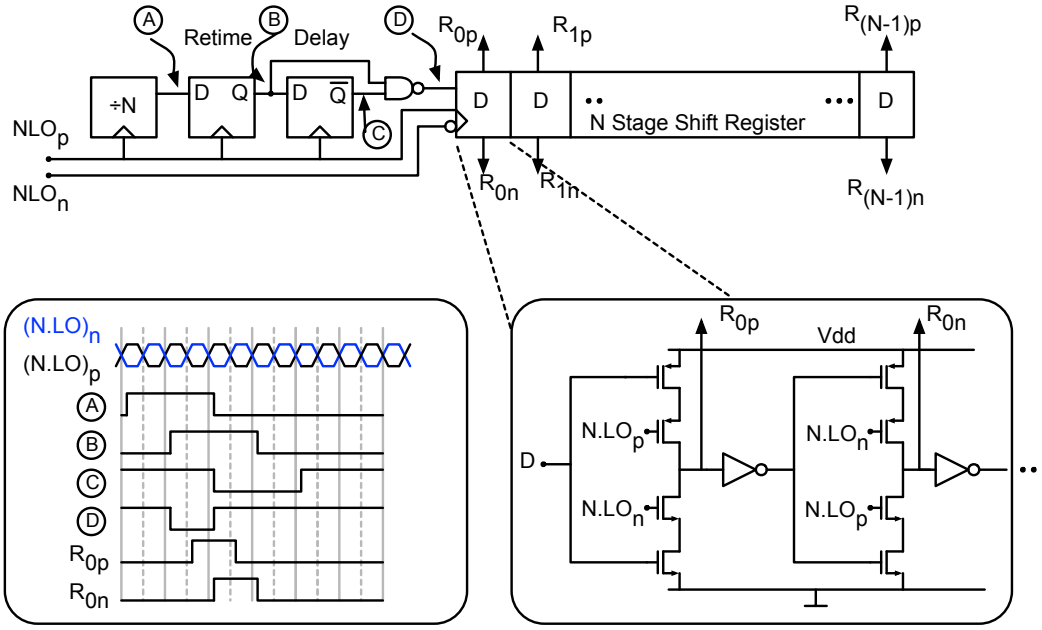


Figure 3.5: Circuit Implementation of Multi-phase LO generation.

(R) provide the low-pass filtering needed for the mixer in Fig. 3.2.

3.2.1 Multi-phase LO generation

Circuit to realize the gating signals for $RP_0 - RP_{N-1}$ and $RN_0 - RN_{N-1}$ is shown in Fig. 3.5. Firstly, the NLO clock is divided by N. The divided output (point A in Fig. 3.5) is retimed and delayed further by a period of NLO clock by a D flip-flop to generate the output C. Outputs B and C are nanded to generate a pulse whose width is one period of the NLO clock. This pulse is then loaded onto a N stage shift register comprised of master-slave dynamic latches as shown. The outputs of master and slave latches drive the gates of $RP_0 - RP_{N-1}$ and $RN_0 - RN_{N-1}$ respectively.

3.3 Non-idealities: Mismatches

Device mismatches in the master LO transistors modulate the pulse widths of instantaneous currents through MP and MN, shown as i_p and i_n, in Fig. 3.2. If the current pulse i_p widens due to mismatches, then i_n narrows by an equal amount. But the sum of i_p and i_n, has the same pulse width as in the case without mismatches. The period of conduction of RF signal current to any IF port and hence the conversion gain, is unaffected by these transistor mismatches. Since the delay caused by mismatches in the time of conduction is the same for every IF output, there is no relative phase shift between signals at any two IF ports (Fig. 3.4). Thus, device mismatches do not cause any phase or gain errors. Gates of rotational transistors are biased such that at the time of conduction, they merely serve as cascodes (Fig. 3.2). This reduces the phase and gain errors caused by mismatches in these transistors.

3.4 IF Section Implementation and Operation

The IF section weights the multi-phase mixer outputs with samples of Cosine and Sine waves and sums them to generate I and Q outputs respectively. The functionality of IF section can be expressed as in (3.1) ,

$$\begin{bmatrix} a_{N/4} & a_{N/4+1} & \dots & a_{N/4-1} \\ a_0 & a_1 & \dots & a_{N-1} \end{bmatrix} \begin{bmatrix} IF_0 \\ IF_1 \\ \vdots \\ IF_{N-1} \end{bmatrix} = \begin{bmatrix} I_{out} \\ Q_{out} \end{bmatrix} \tag{3.1}$$

where $a_k = sin\left(\frac{2\pi k}{N}\right)$ for $k = 0$ to $N-1$. Quadrature phase output

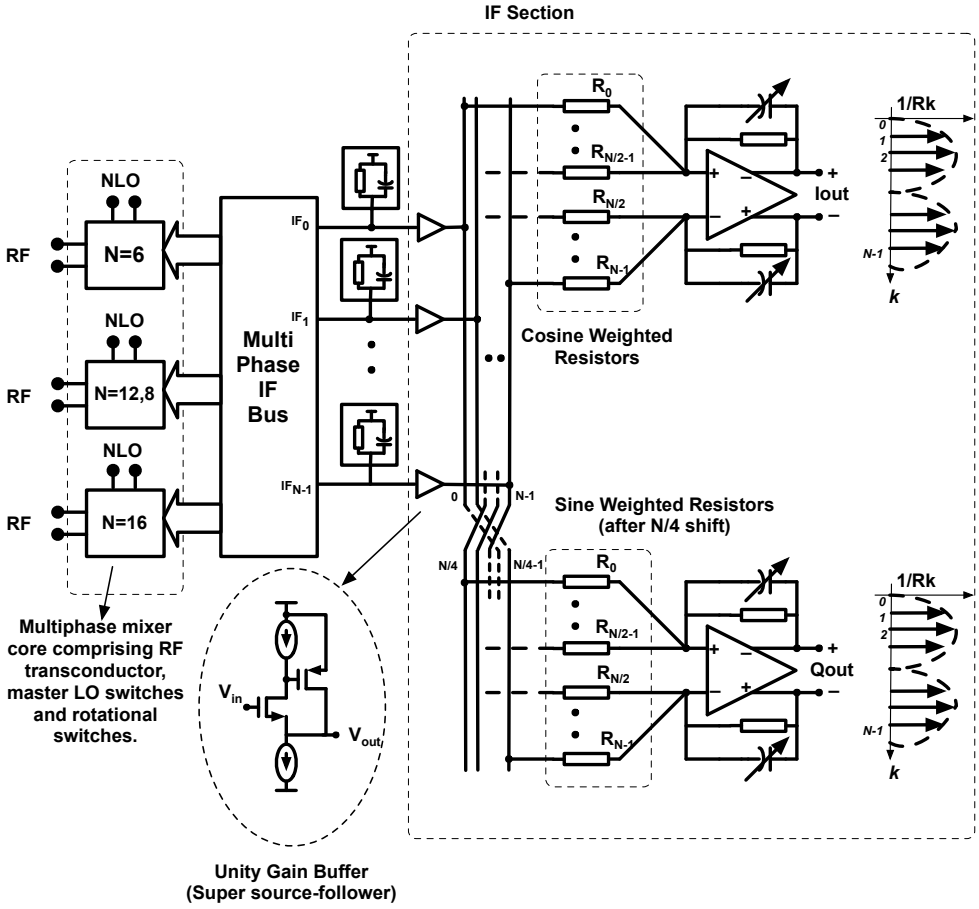


Figure 3.6: Circuit of IF Section.

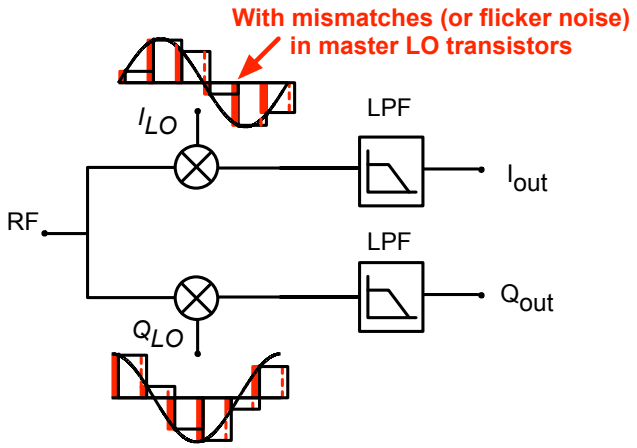


Figure 3.7: A simplified equivalent model for the mixer.

is obtained by using the above sine wave coefficients, shifted by $N/4$. Implementation of the IF section is shown in Fig. 3.6. Multi-phase mixer outputs are buffered through super source-followers. Substantial loop gain is available for negative feedback of this buffer in these unity-gain buffers at the low IF frequency. This significantly reduces gain and phase errors. Gains proportional to sine wave coefficients are set by conductances proportional to sine wave samples.

3.5 Thermal Noise Performance

Noise for this mixer is dominated by the noise of the RF transconductor. The functionality of RF and IF sections can be combined into an equivalent model for the mixer as shown in Fig. 3.7. Signal at the RF port of the mixer is multiplied by an N-step approximation to a cosine (or sine) wave

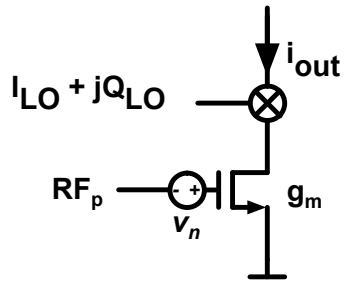


Figure 3.8: Noise of the RF transconductor.

and low-pass filtered to generate the I (or Q) outputs. In order to facilitate the noise analysis of the RF transconductor, a simplified model as shown in Fig. 3.8 is used. The noise of the RF transconductor is modeled as a voltage source in series with the gate of the RF transconductor. Its double-sided power spectral density (PSD) is given by $\hat{v_n^2} = 2kT\gamma\left(\frac{1}{g_m}\right)$, where g_m is the transconductance and γ in the excess noise factor. γ equals 2/3 for long channel MOSFETs [50], but could be higher for shorter channel lengths [51–54]. The RF transconductor's white noise is frequency translated by the harmonics and fundamental of $I_{LO}(t) + jQ_{LO}(t)$. Fourier series expansion of this gives:

$$I_{LO}(t) + jQ_{LO}(t) = \sum_{-\infty}^{\infty} c_n \exp(jn\omega_{LO}t) \tag{3.2}$$

Thus, the noise PSD at the output is higher than the contribution from the fundamental component alone. The noise PSD after multiplication of RF with $I_{LO}(t) + jQ_{LO}(t)$ is given by (3.3). If $\mid I_{LO}(t) + jQ_{LO}(t) \mid = 1$, the term

in parenthesis equals 1 by Rayleigh's energy theorem [55].

$$\hat{i_{out}^2} = 2kT\gamma g_m \times (\sum_{-\infty}^{\infty} \mid c_n \mid^2) = 2kT\gamma g_m \tag{3.3}$$

But the desired signal at the output is only due to the frequency translation from the fundamental. Thus, if the RF input signal voltage is $cos(\omega_{RF}t)$ then after down-conversion and low-pass filtering the current at the output is given by the following equation.

$$i_{out} = gm \cdot \left(\frac{1}{2}\right) exp(j\omega_{IF}t) \cdot sinc\left(\frac{1}{N}\right) \tag{3.4}$$

.

The term $\frac{1}{2}$ in parenthesis is because only either the positive or negative side-band of the RF signal is down-converted to the IF frequency and the term $sinc(\frac{1}{N})$ is the fundamental component of $I_{LO}(t)+jQ_{LO}(t)$. The ratio between the power of the down-converted signal at the output and the power of the RF voltage signal at the input, represents the conversion transconductance due to the fundamental component (G_{meff}).

$$G_{meff}^2 = \frac{\left(\frac{gm}{2} sinc\left(\frac{1}{N}\right)\right)^2}{\left(\frac{1}{2}\right)} \tag{3.5}$$

$$G_{meff}^2 = \frac{g_m^2}{2} \cdot sinc^2\left(\frac{1}{N}\right) \tag{3.6}$$

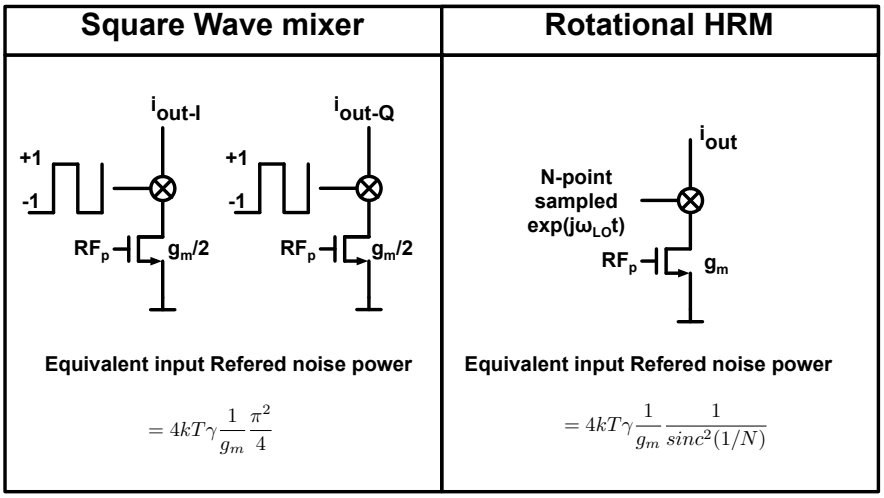


Figure 3.9: Comparison with noise performance of square-wave mixer.

The equivalent input referred noise PSD is obtained by dividing the output noise PSD by the conversion gain only due to the fundamental ($= \frac{g_m^2}{2} sinc^2(\frac{1}{N})$). This results in an equivalent input referred noise PSD of

$$\hat{v_{n-eq}^2} = 4kT\gamma \left(\frac{1}{g_m}\right) \frac{1}{sinc^2(\frac{1}{N})} \tag{3.7}$$

It is insightful to compare this noise, with that of a conventional square-wave mixer of the same total transconductor. A similar analysis shows that for a square-wave mixer with 50% duty-cycle LO as shown in Fig. 3.9, the input referred voltage noise PSD, $\hat{v_{n-eq}^2} = 4kT\gamma \left(\frac{1}{g_m}\right) \frac{\pi^2}{4}$. For $N = 16$, the noise of the proposed mixer is smaller a factor of $\frac{\pi}{4}^2$ or 3.9 dB [23]. 0.9 dB of this difference is because noise of the RF transconductor around the 3^{rd}, 5^{th}, 7^{th}... harmonics gets canceled at the output similar to the RF signal around these

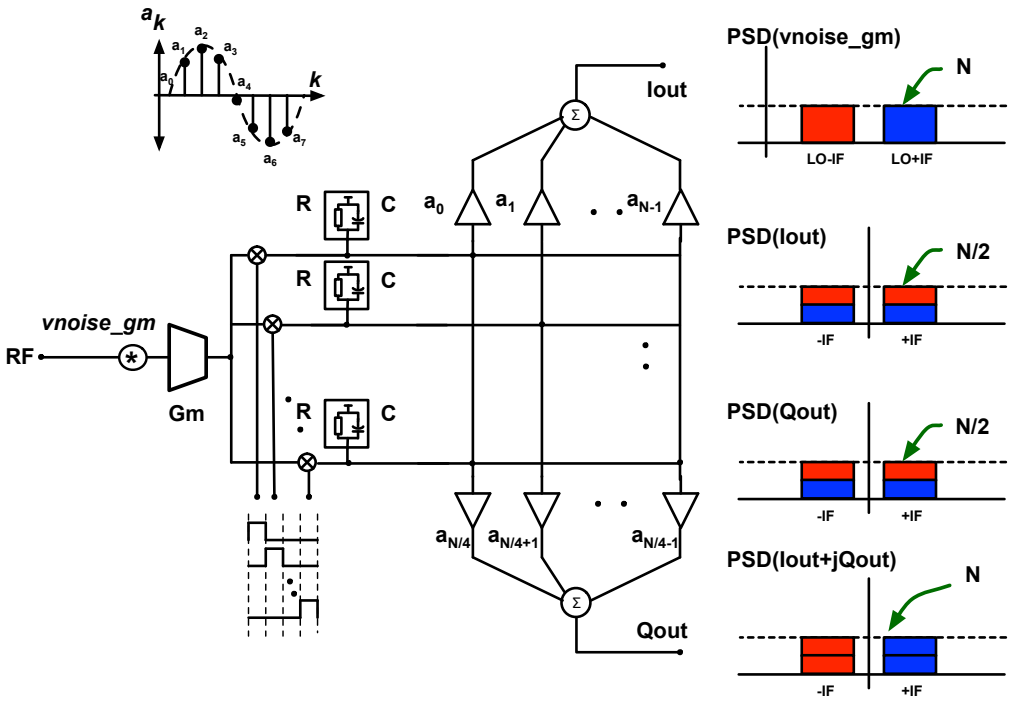


Figure 3.10: Quadrature generation using a single multi-phase mixer.

frequencies. The rest (3 dB) is because the noise of the RF transconductor from the image frequency does not appear at the desired complex IF output.

3.6 Insight into the Thermal Noise Benefit

In order to illustrate the 3 dB benefit outlined in the earlier section, it is useful to look at the two ways quadrature outputs can be generated in harmonic rejection mixers. In Fig. 3.10, a single multi-phase mixers is used. The other approach for generating quadrature using two distinct multi-phase mixers is shown in Fig. 3.11. For the first approach shown in Fig. 3.10, the RF

transconductance used in the multi-phase mixer is G_m. The RF transconductor current is multiplied by $1/N$ duty-cycle rectangular waveforms and passed through low pass filters (R and C) to generate N multi-phase IF outputs. The multi-phase mixer outputs are weighted with samples of cosine ($a_{N/4} \ldots a_{N/4-1}$) and sine ($a_0 \ldots a_{N-1}$) waves to generate I and Q outputs, respectively (I_{out} and Q_{out} in Fig. 3.10). The noise of the RF transconductor is modeled as a voltage source in series with the gate as shown. Upon multiplication with $1/N$ duty cycle waveforms, the RF transconductors noise is frequency translated and appears at I_{out} and Q_{out}. However, the noise from both the desired and image frequencies (LO+IF and LO-IF respectively) appears at each of I_{out} and Q_{out}. But RF transconductor's noise at I_{out} and Q_{out} is correlated with each other. Hence, at $I_{out} + jQ_{out}$ the noise from the image frequency is separated from the desired. If the double sided PSD of noise at I_{out} and Q_{out} is $N/2$, the PSD of noise at $I_{out} + jQ_{out}$ is N.

In order to facilitate comparison, the second approach shown in Fig. 3.11, uses the same total transconductance current. Thus, each of the two multi-phase mixers uses an RF transcondutance of $G_m/2$. Also, the gain of this mixer is kept the same as in the earlier case. Thus, the RF transconductor's current after multiplication with $1/N$ duty-cycle waveforms flows to mixer load comprised of $2R$ and $C/2$. The same sine and cosine weights are used to generate I and Q outputs, as in the earlier case. The voltage noise PSD of each of the RF transconductors is 2X that of the noise PSD of the single RF transconductor in the earlier case. This is because each of the RF

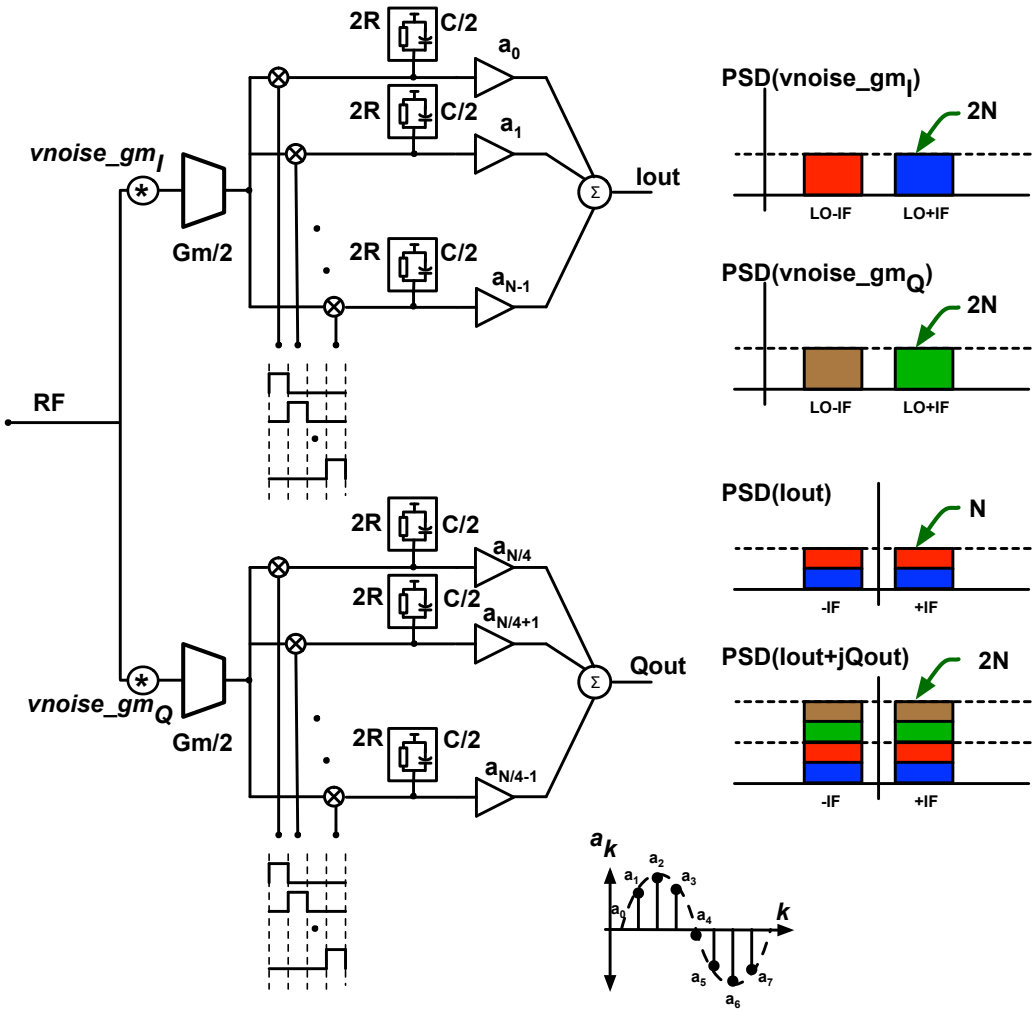


Figure 3.11: Quadrature generation using two distinct multi-phase mixers.

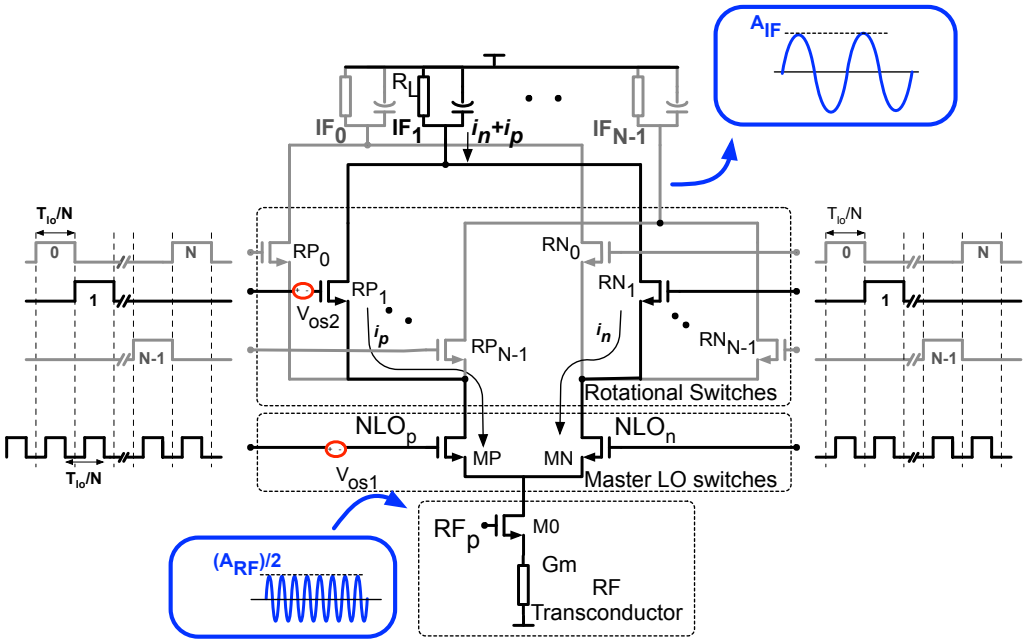


Figure 3.12: Conversion Gain in the RF section of the mixer.

transconductors takes only half the current. Since the gain to each of I_{out} and Q_{out} is the same as in the earlier case, the double sided PSD at I_{out} is N (half of the noise PSD of the RF transconductor as in the earlier case). Since the noise of the two RF transconductors is not correlated, at $I_{out} + jQ_{out}$ the double sided noise PSD is $2N$. This is 2X (or 3 dB) more than the noise of the earlier case despite the same total RF current being used here and the two schemes having identical gains.

3.7 Conversion Gain and IIP3

3.7.1 Gain in the RF section

The conversion gain definition for a multi-phase mixer is ambiguous given that signals are present in different phases at its outputs. It is useful to define the gain as the ratio of the sinusoidal signal amplitude at any of the single ended multi-phase outputs to the sinusoidal signal amplitude at the differential RF input (G_{RF}) . Fig. 3.12 shows a single balanced mixer with signals at the RF and IF port of the mixer. Since the actual implementation is double balanced, the peak signal at the input of the RF transconductor is half of the differential peak.

$$G_{RF} = \frac{A_{IF}}{A_{RF}} \tag{3.8}$$

The RF current in the transconductor is effectively multiplied by $1/N$ duty-cycle rectangular waveforms, as shown in section 3.2. Thus, the IF signal obtained after frequency translation is related to the RF input in accordance with (3.10) below. $G_m$refers to the transconductance of the RF transconductor and $R_L$is the load resistance. The term in square parenthesis is the fundamental component of the $1/N$ duty-cycle multiplying waveform.

$$A_{IF}cos(\omega_{IF}t) = \frac{A_{RF}}{2}cos(\omega_{RF}t)G_mR_L\left[\frac{2}{N}sinc(\frac{1}{N})cos(\omega_{LO}t)\right] \tag{3.9}$$

$$G_{RF} = G_m\frac{R_L}{N}sinc(\frac{1}{N}) \tag{3.10}$$

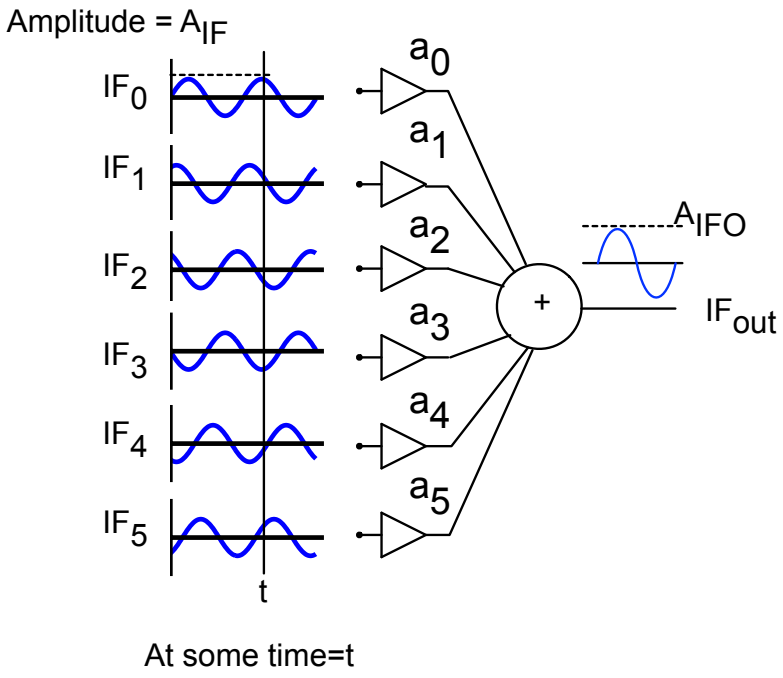


Figure 3.13: Conversion Gain in the IF section of the mixer.

In this design, for $N = 16$, G_{RF} is about 6 dB. To put this in perspective, signals at IF_0, IF_4, IF_8 and IF_{12} have 0^o, 90^o, 180^o and 270^o as their relative phases respectively. At $IF_0 - IF_8$ and $IF_4 - IF_{12}$, we have quadrature outputs similar to a Gilbert-cell type active square-wave quadrature mixer. Complex signal at this quadrature output has an equivalent gain of 15 dB (= 6 + 6 + 3 dB) from the differential RF port of the mixer. This is a reasonable gain for a power supply of 2.7 V and mixer IIP3 of 12 dBm.

3.7.2 Gain in the IF section

IF section weights the multi-phase mixer outputs with samples of cosine and sine waves to generate I and Q outputs respectively as per 3.1. The realization of one of I (or Q) outputs is shown in Fig. 3.13 for the case of $N = 6$. To be consistent with the RF section, the Gain in the IF section (G_{IF}) is defined as the ratio of sinusoidal signal amplitude after the sine-weighted sum (A_{IFO}) to the sinusoidal signal amplitude at any of the multi-phase mixer outputs (A_{IF}). Thus,

$$GIF = \frac{A_{IFO}}{A_{IF}} \tag{3.11}$$

At time t,

$$\sum_{k=0}^{N-1} v(IF_k)a_k = v(IF_{out}). \tag{3.12}$$

The phase shift between adjacent IF outputs is $\frac{2\pi}{N}$. So the samples of $v(IF_k)$ lie on a sine wave that completes one period on the k axis ($k = 0$ to $k = N-1$). Using (3.12), we have

$$\sum_{k=0}^{N-1} A_{IF} sin\left(\frac{2\pi k}{N} + \theta\right) a_{kmax} sin\left(\frac{2\pi k}{N}\right) = v(IF_{out}) \tag{3.13}$$

where θ is the phase of $v(IF_0)$ at time t and is function of time and a_{kmax} is the maximum value of a_k. The maximum of $v(IF_{out})$ occurs for $\theta = 0$ and equals A_{IFO}. Thus,

$$A_{IF} \cdot a_{kmax} \cdot \frac{N}{2} = A_{IFO} \tag{3.14}$$

$$G_{IF} = a_{kmax}\frac{N}{2}. \tag{3.15}$$

The complex gain of the mixer including both the gains in the RF and IF sections is 3 dB higher than the product of G_{RF} and G_{IF}. This is because the signal at the quadrature outputs adds to the desired signal power by 3 dB. This is given by3.16

$$G_{tot} = \sqrt{2} \cdot G_{RF}G_{IF} = \sqrt{2}G_m R_L sinc(\frac{1}{N})a_{kmax} \tag{3.16}$$

For different values of N, the complex gain (G_{tot}) has only a small variation if by design $a_{kmax}R_L$ is roughly kept a constant.

3.7.3 IIP3

IIP3 for this mixer is largely determined by the RF transconductor. Source degeneration is used to achieve better IIP3 for the same available gate over-drive voltage. The pole frequency at the common-source of the rotational transistors is greater than 5 GHz and has a negligible effect on the overall linearity of the mixer.

3.8 Flicker Noise Upconversion

Techniques to cancel flicker noise in active square-wave LO mixers through dynamic current injection [56] and as common-mode [57] have been presented. In this mixer, flicker noise cancels at the single-ended output.

Flicker noise of the master LO transistors (Fig. 3.2) can be modeled as a slowly varying voltage source in series with the gate. Similar to the effect of device mismatches in master LO transistors, flicker noise does not affect the duration of current flowing into any IF output. Hence, the average value of the current flowing into any IF output is not affected. This rejects flicker noise at the single-ended IF output for this mixer. However, as shown in the Fig. 3.2, the switching instant of the master LO differential pair is altered by the instantaneous value of flicker noise. If $v_{nf}(t)$ represents the instantaneous value of flicker noise modeled as a voltage source in series with the gate, then switching instant changes by $\Delta t = \frac{v_{nf}(t)}{S}$, where S is the slope of the differential NLO clock. Equivalently, as shown in Fig. 3.7, flicker noise of the master LO transistors modulates the phase of effective LO waveform or in other words it appears as LO phase noise. Simulations show that for a slope, S, of 30 GV/s and at an LO frequency of 300 MHz, the phase noise arising from the flicker noise in master LO transistors is much smaller than -160 dBc/Hz at 1 kHz offset. For TV applications, the low frequency phase noise is dominated by contributors from the frequency synthesiser generating LO and contribution from this mechanism is negligibly small. Rotational switches do not add flicker noise as they act as mere cascodes. For this design, flicker noise is dominated

by devices in the IF section. But large device areas can be used at relatively small bandwidth penalty in applications where low flicker noise is critical.

3.9 IIP2 and IR

IIP2 for a mixer is measured by applying two tones at the RF input of the mixer at frequencies, f_1 and f_2. These tones generate an intermodulation component, $IM2$, due to the second order non-linearity in the mixer's RF transconductor or due to self-mixing, at a frequency of $f_1 - f_2$ [58, 59]. This IM2 component appears as common mode current in the RF transconductors. In commutating active mixers, device mismatches in the switching pair and/or load resistor mismatches cause the common mode IM2 component to appear at the differential output [58]. This is one of the dominant IM2 degrading mechanism. For this mixer, however, mismatches in the master LO transistors do not affect the DC component of the $1/N$ duty cycle multiplying waveforms in Fig. 3.4. Rotational switches function as mere cascodes. Thus, at each of the single ended IF outputs, the IM2 component generated in the RF transconductor appears uncorrupted by transistor mismatches in the RF section of the mixer. This IM2 component appears differentially at the output of the IF section due to the mismatches amongst the N mixer load resistors/capacitors and/or mismatches in the sine/cosine weighed resistors. By using large resistor areas in the low frequency IF section, superior IIP2 performance is achieved.

Signal applied to the RF port of the mixer at a frequency of $LO + IF$ is downconverted by the fundamental component of the $1/N$ duty-cycle

multiplying waveform as shown in Fig. 3.4. After down-conversion it appears at a frequency of IF with a phase of 0, $\frac{2\pi}{N}$, $\cdots$ $\frac{(N-1)2\pi}{N}$ at the outputs IF_0, IF_1, $\ldots IF_{N-1}$, respectively. Mismatches in the master LO transistors or rotational transistors do not affect the conversion gain or the relative phase between down-converted signals at any two IF outputs ($IF_0 - IF_{N-1}$). The multi-phase IF outputs are cosine (or sine) weighted and summed to generate I_{out} (or Q_{out}) as per (3.1). Ideally, signals at I_{out} and Q_{out} are in quadrature. The gain/phase relationship between signals at I_{out} and Q_{out} is affected by mismatches in mixer's load resistors/capacitors or in the sine/cosine weighted resistors. Large resistor areas in the IF section achieves superior IR performance.

3.10 HR Performance

Given the reduced sensitivity to mismatches in the RF section, the HR performance is primarily determined by the precision of mixer's RC loads and the sine/cosine weights, both implemented in the low frequency IF section. A key benefit of this mixer, is that larger resistor areas can indeed be used to enable better matching without paying a power or RF bandwidth penalty.

There are three components to achieving a high degree of HR performance. Firstly, the systematic HR of the mixer should be high. Secondly, the permissible random variation in sine weights arising from resistor mismatches is determined by the performance specification of the system. Finally, the total area is optimized by the allocation of area to mixer's load resistors and sine/cosine weighted resistors.

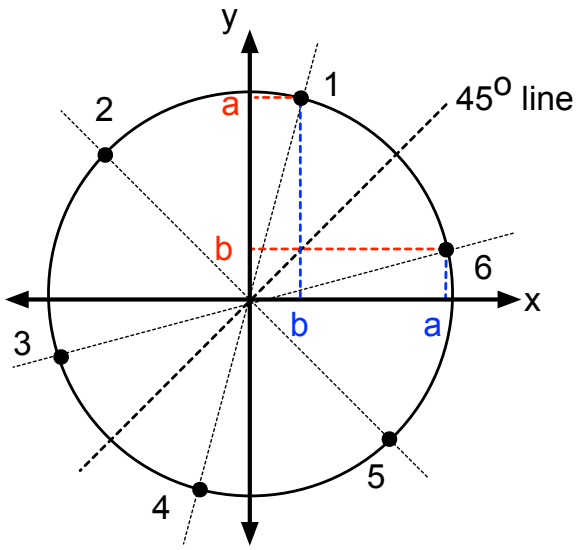


Figure 3.14: Sine/Cosine weights for N=6.

3.10.1 Systematic HR

The systematic component for HR is controlled by the precision of the sine/cosine coefficients used to weight the multi-phase IF signals. Any deviation from an ideal sine wave degrades systematic HR. A reasonable target to use is to set it at the level where second order and layout dependant effects start manifesting. In this design, the sine weights were chosen in order to have a systematic HR better than 60 dB for all harmonics.

Ideally, if infinite precision was available in the implementation of sine / cosine weights, then for any value θ, $cos(\frac{2\pi k}{N} + \theta)$ and $sin(\frac{2\pi k}{N} + \theta)$ yield perfect I and Q weights respectively for $k = 0 \ldots N - 1$. However, in a practical implementation the sine and cosine weights will have finite precision. It is

N	Half sine weights	Half cosine weights
6	$[17\ 23\frac{1}{5}\ 6\frac{1}{5}]$	$[17\ -6\frac{1}{5}\ -23\frac{1}{5}]$
8	[0 17 24 17]	[24 17 0 −17]
12	$[6\frac{1}{5}\ 17\ 23\frac{1}{5}\ 23\frac{1}{5}\ 17\ 6\frac{1}{5}]$	$[\ 23\frac{1}{5}\ 17\ 6\frac{1}{5}\ -6\frac{1}{5}\ -17\ -23\frac{1}{5}]$
16	$[0\ 9\frac{1}{5}\ 17\ 22\frac{1}{5}\ 24\ 22\frac{1}{5}\ 17\ 9\frac{1}{5}]$	$[\ 24\ 22\frac{1}{5}\ 17\ 9\frac{1}{5}\ 0\ -9\frac{1}{5}$ -17 $-22\frac{1}{5}\ ]$

Table 3.1: Sine/Cosine Weights.

desirable that sine and cosine weights are generated from the same set of values so that the systematic HR is the same on I and Q sides. Also, this will ease the implementation as layouts can be shared between the I and Q sides. Hence the following methodology is used for choosing sine/cosine weights: As shown in Fig. 3.14 for the case of $N = 6$, N equally spaced points are chosen symmetrically about a 45^o line on a unit circle. The X and Y co-ordinates of these points are the cosine and sine weights respectively. For every pair of points symmetrical about the 45^o line, the X and Y co-ordinates are from the same set of values. Using this approach when N is a multiple of 4 gives cosine weights that are N/4 shifted with respect to the sine weights. But even when N is not a multiple of 4, this approach still yields sine/cosine weights that are in quadrature using the same set of values as shown in Fig. 3.14. The sine/cosine weights used in this design for N =6, 8, 12 and 16 are summarized in Table 3.1.

The sine/cosine weights are implemented as conductances as shown in

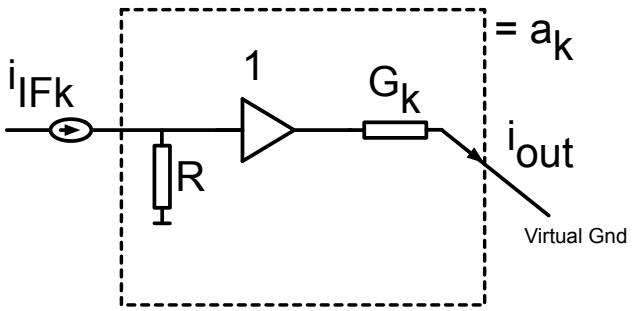


Figure 3.15: Implementation of a sine weight a_k.

Fig. 3.6 ($1/R_k$ for $k = 0 \ldots N-1$). In order to avoid end effects in resistors, the same unit resistor is used for the implementation of all sine/cosine weights. The integer part represents the number of unit resistors in parallel while the fractional part represents the number of unit resistors in series, used in the implementation of sine weights.

3.10.2 Random HR

Random mismatches in the mixer's load resistors (R in Fig. 3.2) and in the conductances between the unity gain buffer and the virtual ground of opamp on I (or Q) side ($1/R_k$ in Fig. 3.6), causes a deviation in the value of sine weights. Fig. 3.15 shows the implementation of a sine weight. Here, i_{IF_k}represents the current flowing into any particular IF output IF_k and i_{out} represents the weighted current flowing into the virtual ground of the opamp. R is the mixer's load resistor and G_k is $1/R_k$ as discussed above. Thus,

$$a_k = \frac{i_{out}}{i_{IF_k}} = \frac{G_k}{R} \tag{3.17}$$

The deviation in a_k is related to the deviations in the value of G_k and R according the following equation.

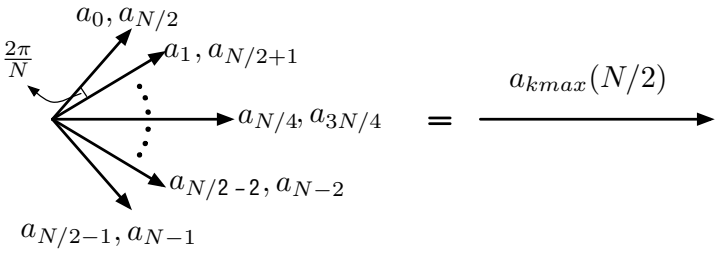
$$\frac{\Delta a_k}{a_k} = \frac{\Delta G_k}{G_k} + \frac{\Delta R}{R} \tag{3.18}$$

As per Pelgrom's model for random device mismatches [60, 61], the standard deviation of the mismatch in the value of resistance is related to the area of the resistor as shown below:

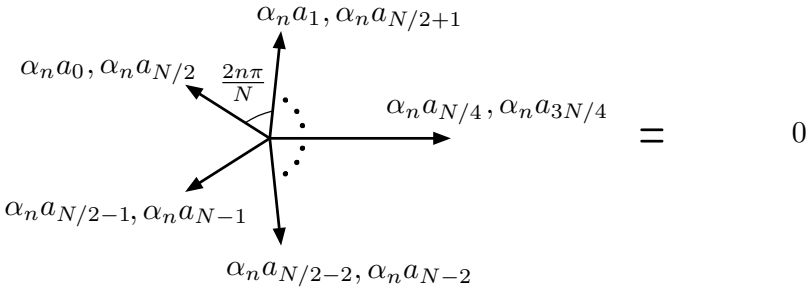
$$\frac{\sigma_{\Delta R}}{R} \propto \frac{1}{\sqrt{Area}} \tag{3.19}$$

Thus, the use of larger resistor area reduces the random deviation in the value of a sine weight. But semiconductor area is a precious resource. If most of the available area is allocated to mixer's load resistance (R), then less area is available for the implementation of G_k. This will result in a higher value of $\frac{\Delta Gk}{Gk}$ and cause $\frac{\Delta a_k}{a_k}$ to be higher despite $\frac{\Delta R}{R}$ being small. And vice-versa is also true. Thus, the allocation of available area between the mixer's load resistor, R, and G_k will determine the relative error in a sine weight. Furthermore, the relative error in one of the sine weights might not have the same effect on the HR performance as the same relative error on another sine weight. Hence, in order to allocate the area efficiently we will first need to understand, how the HR performance is affected by a given relative error in a particular sine weight.

Fig.3.16 shows the sine weighted signals in phasor notation. In (a) signals down-converted by the fundamental component is shown and (b) shows



(a)



(b)

Figure 3.16: Sine weighted signals in Phasor Notation (a) Fundamental Component and (b) n^{th} Harmonic.

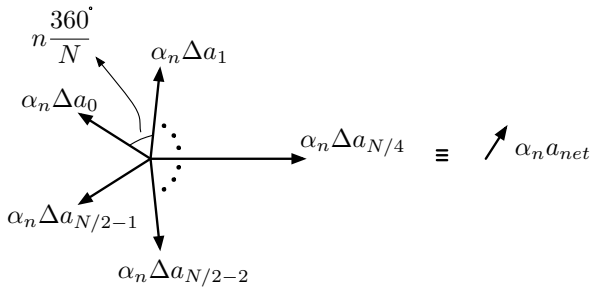


Figure 3.17: In the presence of mismatches

the signals for the nth harmonic down-conversion. For the signals shown in (a), the angle between adjacent phasors is $\frac{2\pi}{N}$ radians. Since the phase shift between IF_k and $IF_{k+N/2}$ is π radians, the phasor corresponding $IF_{k+N/2}$ lies underneath the phasor of IF_k. As seen in Fig. 3.16, the horizontal components of all the phasors add while the vertical components cancels. It can be shown that the resultant of these phasors is $a_{kmax}.\left(\frac{N}{2}\right)$. For signals down-converted by the nth harmonic, the phase shift between signals at adjacent IF outputs is $n\left(\frac{2\pi}{N}\right)$. This causes the phasors to diverge away from each other. When $n \neq N \pm 1$, the phasors cancel perfectly if the sine weights are ideal. Also, each phasor is scaled by α_n. It represents the ratio of the n^{th} harmonic of a $1/N$ duty cycle rectangular waveform to the fundamental component, as shown below:

$$\alpha_n = \frac{sinc\left(\frac{n}{N}\right)}{sinc\left(\frac{1}{N}\right)} \tag{3.20}$$

When the sine weights deviate from their ideal values, the phasors no longer cancel perfectly and a residue is present as shown by $\alpha_n\Delta a_{net}$ in

Fig. 3.17. This results in finite rejection of the signals down-converted by the n^{th} harmonic. Harmonic Rejection Ratio (HR_n) is defined as the ratio between the desired signal down-converted by the fundamental component to the signal down-converted by the nth harmonic, when the same RF signal power is applied around both. From Figs. 3.17 and 3.16,

$$HRn = \frac{\alpha_n \cdot a_{net}}{a_{kmax} \cdot \left(\frac{N}{2}\right)}. \tag{3.21}$$

An interesting observation here is for the hypothetical case when all sine weights are perfect except for one with an index of m. An absolute deviation Δa in this sine weight produces the same HR_n independant of m. In other words, the same absolute deviation in any of the sine weights produces the same HR ratio. This is interesting because, for the same absolute deviation, the sine weights at the peak of the sine wave have a smaller relative error ($\frac{\Delta a_k}{a_k}$) than the rising/falling portions of the sine wave. In other words, for the same percentage error, the sine weights at the peak cause a worse HR ratio than the weights in the rising/falling portions of the sine wave. Since, the area occupied by a resistor determines the standard deviation of the relative error as per (3.19), it is better to use larger resistor areas at the peaks of the sine wave than at the rising/falling portions. In this design, sine weights as shown in Table 3.1 are used. The same unit resistor is used in the implementation of all sine weights. The integer part is realized using unit resistors in parallel. This naturally results in larger resistor areas for the weights at the peaks of the sine wave than at the rising/falling portions.

Rewriting (3.18) in terms of the standard deviations,

$$\frac{\sigma^2_{\Delta a_k}}{a_k^2} = \frac{\sigma^2_{\Delta R}}{R^2} + \frac{\sigma^2_{\Delta G_k}}{G_k^2} \tag{3.22}$$

If ΔG_k is implemented as a_k units of unit conductance G_u in parallel, we have

$$\sigma^2_{\Delta a_k} = a_k^2 \cdot \left(\frac{\sigma_{\Delta R}}{R}\right)^2 + \mid a_k \mid \cdot \left(\frac{\sigma_{\Delta G_u}}{G_u}\right)^2 \tag{3.23}$$

For $\theta_k = 2\pi k/N$,

$$\Delta a_{net} = \sum_{k=0}^{N-1} \Delta a_k exp(j\theta_k) \tag{3.24}$$

$$E\left[\mid \Delta a_k \mid^2\right] = E\left[\left(\sum_{m=0}^{N-1} \Delta a_m exp(j\theta_m)\right)\left(\sum_{n=0}^{N-1} \Delta a_n exp(-j\theta_n)\right)\right]$$

$$= E\left[\sum_{m}^{N-1}\sum_{n}^{N-1} \Delta a_m \Delta a_n exp(j\theta_m)\left(exp(-j\theta_n)\right)\right]$$

But for $m \neq n$, $E\left[\Delta a_m \Delta a_n\right]$=0 as Δa_m and Δa_n are independent zero-mean random variables. After elimination of the cross-terms

$$E\left[\mid \Delta a_{net} \mid^2\right] = E\left[\sum_{k=0}^{N-1} \Delta a_k^2\right] \tag{3.25}$$

$$E\left[HR_n^2\right] = \left(\frac{\alpha_n}{a_{kmax}\cdot\left(\frac{N}{2}\right)}\right)^2 E\left[\sum_{k=0}^{N-1}\left\{a_k^2\cdot\left(\frac{\sigma_{\Delta R}}{R}\right)^2 + a_k\cdot\left(\frac{\sigma_{\Delta G_u}}{G_u}\right)^2\right\}\right] \tag{3.26}$$

In this design, contribution to the harmonic rejection ratio from the mixer's load resistor was made equal to the contribution from the conductance between the unity gain buffer and the virtual ground of the opamp. This leads to

$$\frac{\sigma_{\Delta R}}{R} = \frac{\sigma_{\Delta G_u}}{G_u}\sqrt{\frac{\sum a_k^2}{\sum \mid a_k \mid}} \tag{3.27}$$

$$\frac{Area_R}{Area_{Gu}} = \frac{\sum a_k^2}{\sum \mid a_k \mid} \tag{3.28}$$

For N=16 and for the weights shown in Table 3.1, the ratio of $\frac{\sum a_k^2}{\sum |a_k|}$ equals 19. Therefore, the area of the unit resistor used in implementing sine/cosine weights was chosen to be 19 times smaller than the area of mixer's load resistor. The overall area consumed by mixer's load resistance was 0.008 mm^2 and the sine/cosine weighted resistors occupied 0.026 mm^2.

3.10.3 Layout Considerations

Layout is critical to ensure that the implemented sine/cosine weights are indeed close enough to an ideal sine wave. For instance, unaccounted routing resistances between the unity gain buffer and the virtual ground of the opamp can change the value of a sine weight and hence reduce the systematic HR. Also, parasitic crosstalk between the multi-phase mixer outputs should

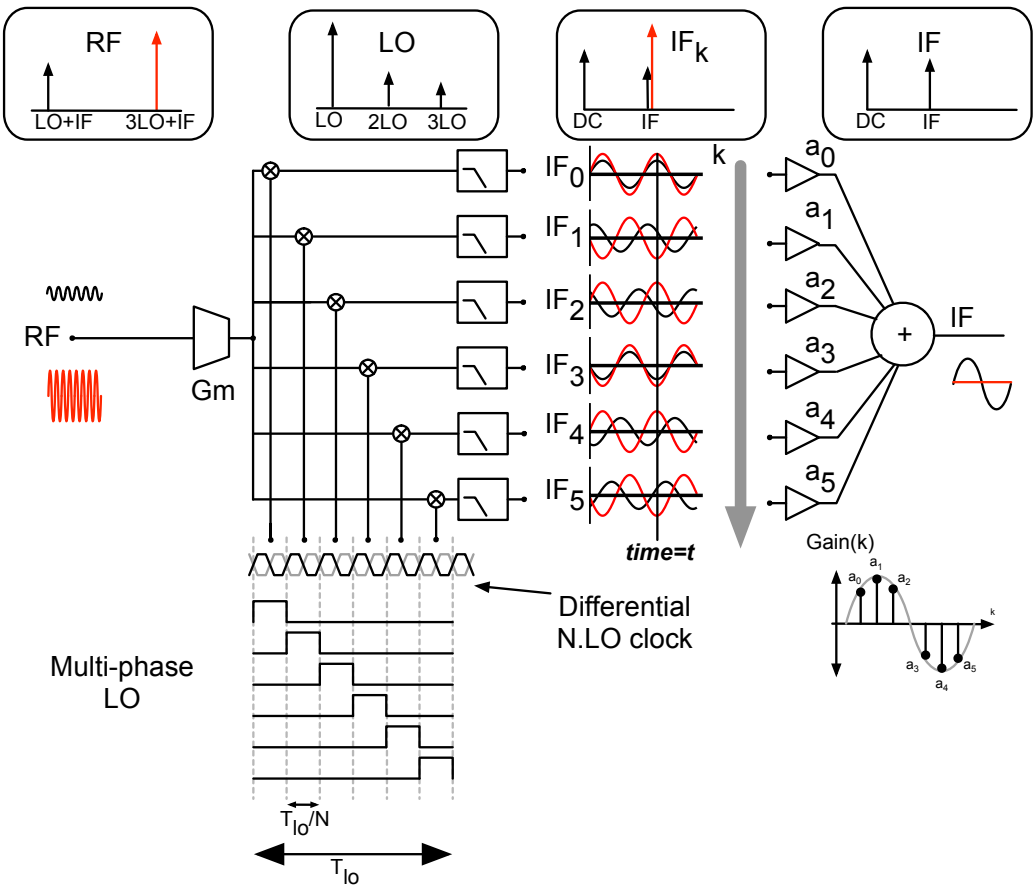


Figure 3.18: Signals in the HRM with N=6.

be kept to a minimum through good shielding as this influences the ideal gain/phase relationship between the multi-phase mixer outputs.

3.11 HR Insight in Space Domain

It is insightful to look at the achievement of harmonic rejection in space domain. Fig. 3.18 shows the signals in a single balanced HRM with $N = 6$ for

clarity. At the RF input of the mixer, desired signal exists at a frequency of $LO + IF$ along with a blocker at a frequency of $3LO + IF$. RF currents at the output of the transconductor are multiplied by time-shifted rectangular waveforms, each of duty cycle 1/6. The time shift between adjacent multiplying waveforms in $T_{LO}/6$. Since these multiplying waveforms are made of pulses of small duty cycle, they are rich in their harmonic content. Upon multiplication of RF with multi-phase LO, the desired RF signal is frequency translated by the fundamental component of the multiplying LO waveform whereas the blocker gets frequency translated by the 3^{rd} harmonic of the rectangular waveform. The blocker and the desired signal appear at the same IF frequency at the outputs of the low-pass filters on $IF_0 - IF_{N-1}$, as shown in Fig. 3.18. The phase shift between adjacent IF outputs is given by (3.29).

$$\angle IF_{p,k+1} - \angle IF_{p,k} = p \cdot \frac{2\pi}{N} \tag{3.29}$$

Thus, for the case of $N = 6$, the phase shift between adjacent IF outputs for the desired signals is $2\pi/6$, whereas for the blocker down-converted by the 3^{rd} harmonic, it is three times as much and equals π. The multi-phase IF signals are weighted by weights proportional to sine wave samples and summed to produce the IF output.

In the space domain (along k axis) and at any given time= t, the signal at IF in Fig. 3.18 can be written as follows

$$\sum_{k=0}^{N-1} v(IF_k)a_k = v(IF) \tag{3.30}$$

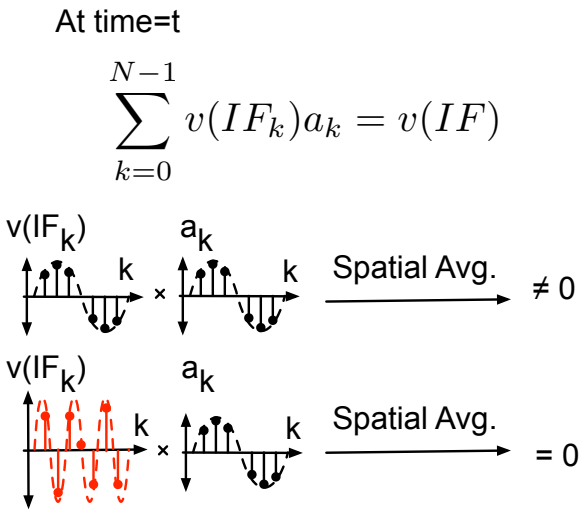


Figure 3.19: Harmonic Cancellation in Space Domain.

For the desired down-converted signal, the samples of $v(IF_k)$ at any time= t lie on sine wave that completes one period along the spatial axis ($k = 0$ to $k = N - 1$). This is illustrated in Fig. 3.19. However, the samples of the blocker at any given time= t, lie on a sine wave that completes three periods along the spatial axis. This is due to the fact that the phase shift between adjacent IF outputs for the blocker is three times as that of the desired signal. Weighting the signals at $IF_0 - IF_{N-1}$ by values proportional to sine wave samples is equivalent to multiplication in the space domain. But since sine waves of two different frequencies are orthogonal, the blocker is canceled after the sine weighted sum. This is shown in Fig. 3.19 and in Eqn. 3.31, where the left hand side equals zero for a positive integer $q \neq 1$ and $q < N - 1$.

$$\sum_{k=0}^{N-1} sin\left(\frac{2k\pi}{N}\right) sin\left(q\frac{2k\pi}{N}\right) = 0 \tag{3.31}$$

3.12 Merits and Demerits

A key advantage of this HR mixing technique is the reduced phase error in multi-phase LO generation. Due to the reduced sensitivity to mismatches in the master LO switching pair and rotational switches, HR performance is primarily determined by resistor/capacitor matching in the low frequency IF section and this enables higher HR performance. This technique thus achieves over 52 dB of 3^{rd} harmonic rejection. Furthermore, mismatches in master LO transistors and rotational switches do not affect the conversion gains or the relative phase between any of the multi-phase IF outputs, for any of the frequency translations associated with the mixing of RF with $1/N$ duty cycle multiplying waveforms. This translates to better IIP2 and IR performance as discussed above. In order to realize the benefit of reduced sensitivity to mismatches in rotational and master LO transistors, it is important that signals at the gates of rotational transistors transition when there is no current in them. Simulations of 16-phase mixer at a NLO clock of 1.6 GHz show that it is possible to guarantee this across PVT variation. The main drawback of this technique is that a larger power supply voltage is needed to accommodate the rotational transistors.

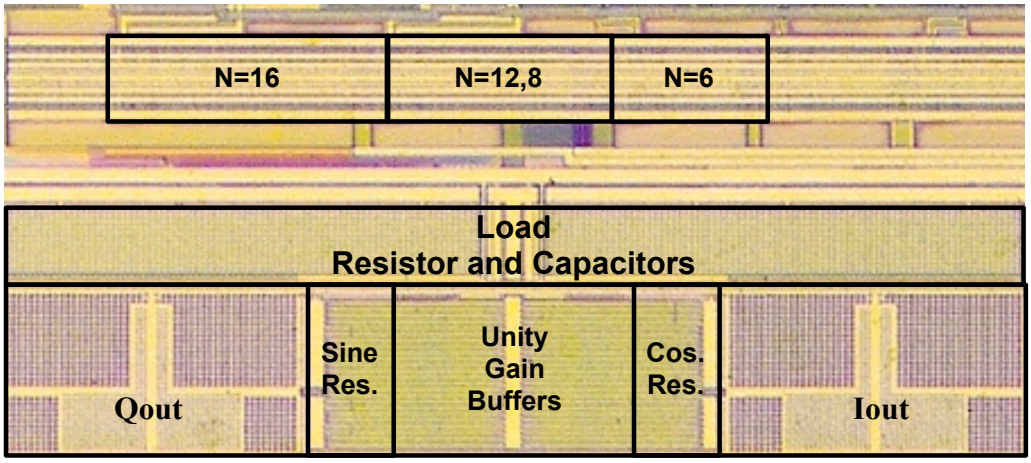


Figure 3.20: Die Photo of N-phase HRM with NLO Clock.

3.13 Measurements and Discussion

This mixer is fabricated in 110 nm CMOS process (Fig. 3.20) as part of a receiver. Multi-phase mixer and unity gain buffers draw 10 mA and 12 mA respectively from 2.7 V. Multi-phase rotational pulse generation and master clock buffering consumes 8 mA from 1.3 V with a master clock of 1.6 GHz in 16-phase mode. Less digital current is consumed for lower N. The measured IIP3 and DSB NF of the mixer extrapolated from the receiver measurements are 12 dBm and 11 dB respectively. The multi-phase mixer load resistors occupy 0.008 mm^2 and the sine/cosine-weighted resistors with switches, 0.026 mm^2.

The measured HR ratios are summarized in Figs. 3.21, 3.22, 3.23 and 3.24. For the n^{th} HR, the rejection is measured with RF signal applied at both

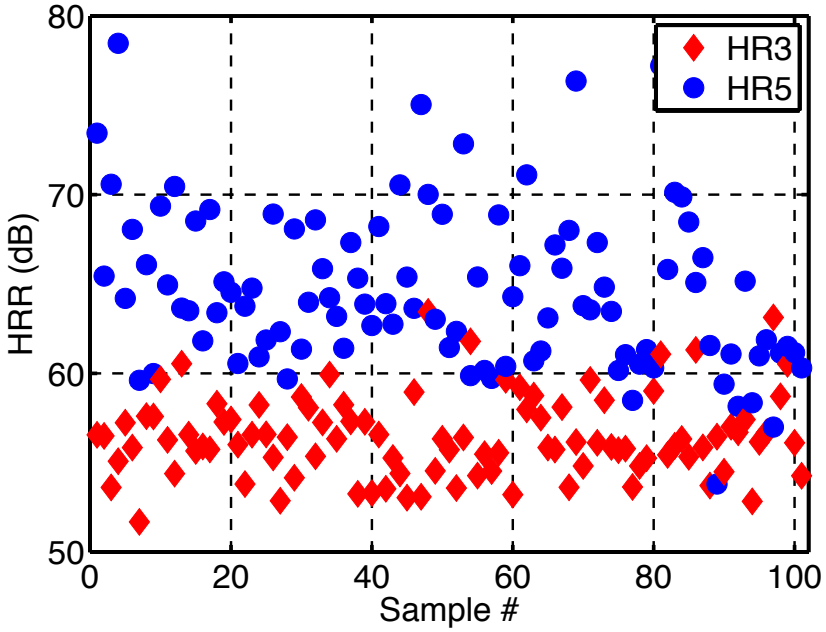


Figure 3.21: HR3 and HR5 for N=8 at LO=200MHz

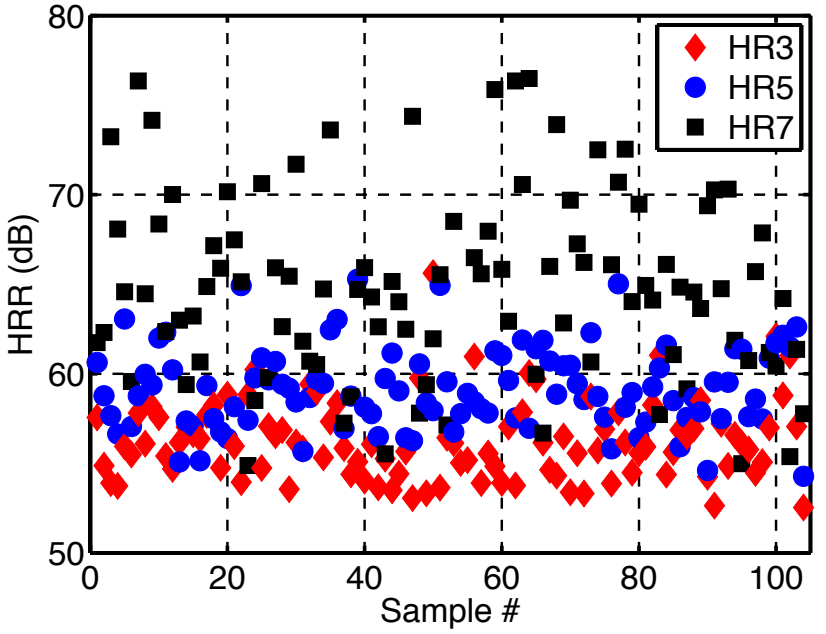


Figure 3.22: HR3, HR5 and HR7 for N=12 at LO=150 MHz

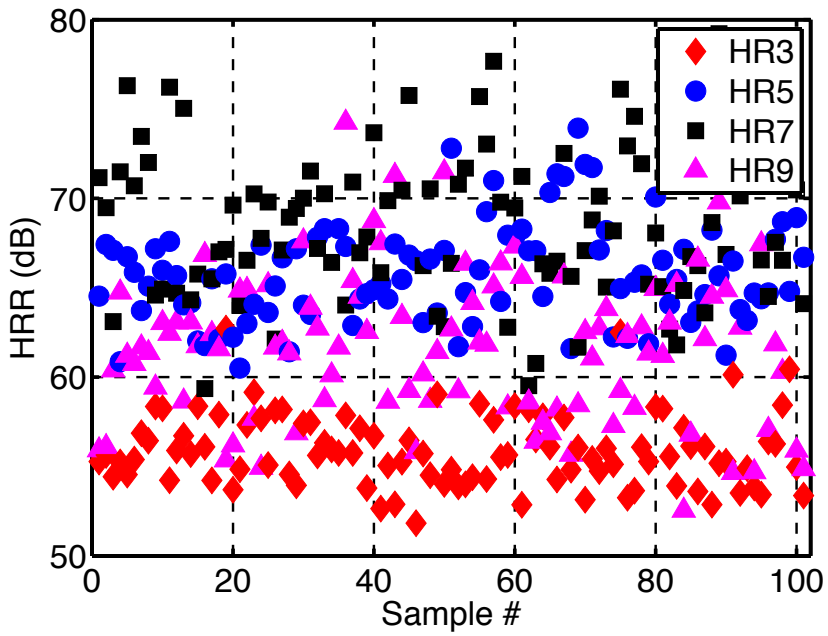


Figure 3.23: HR3, HR5, HR7 and HR9 for N=16 at LO=100 MHz

$nLO + IF$ and $nLO - IF$ frequencies, and the worse of the two rejections is shown. For $N = 8$ and at $LO = 200MHz$, the 3^{rd} and 5^{th} HR ratios are greater than 52 dB and 54 dB respectively, measured over at least 100 parts. For $N = 12$ and at $LO = 150MHz$, the 3^{rd}, 5^{th} and 7^{th} HR ratios are greater than 52, 54 and 55 dB respectively. For $N = 16$ and $LO = 100MHz$, the 3^{rd}, 5^{th}, 7^{th} and 9^{th} HR ratios are respectively greater than 52, 60, 59 and 52 dB. In summary the 3^{rd} HR ratio for N=6, 8, 12 and 16 is greater than 52 dB as shown in Fig. 3.24 without any calibration or trimming. The HR measurements are summarized in the table shown in Fig. 3.25. For analog and digital TV systems, HR in excess of 70 dB is needed. Achievement of greater than 52 dB rejection of the 3^{rd} harmonic implies that the pre-mixer filter needs

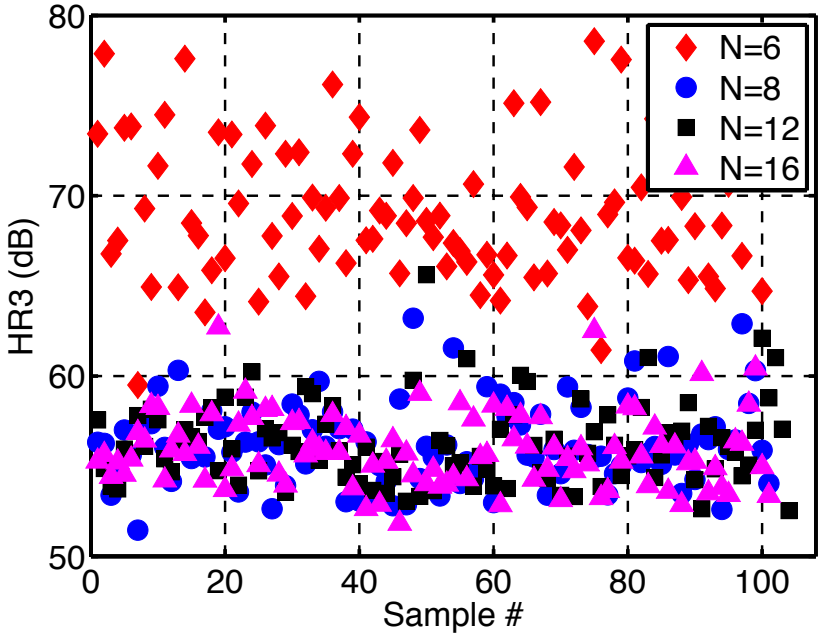


Figure 3.24: HR3 for N=6,8,12 and 16

Statistical Harmonic Rejection Summary (>100 samples)							
N	LO Frequency	Clock Frequency	First Unrejected Harmonic Frequency	HR3	HR5	HR7	HR9
6	300 MHz	1.80 GHz	1.50 GHz	>59dB	-	-	-
8	200 MHz	1.60 GHz	1.40 GHz	>52dB	>54dB	-	-
12	150 MHz	1.80 GHz	1.65 GHz	>52dB	>54dB	>55dB	-
16	100 MHz	1.60 GHz	1.50 GHz	>52dB	>60dB	>59dB	>52dB

Figure 3.25: Tabular Summary of HR performance of N-phase HRM with NLO Clock.

to attenuate the blocker around the 3^{rd} LO harmonic only by 18 dB. This is a considerably simpler requirement for an integrated tuner solution.

It is insightful to take a closer look at distribution of measured HR. While the distribution of parts is spread over a wider range for certain harmonics, for others it is not. For example, in Fig. 3.21, the third harmonic rejection is spread between 52-60 dB for most parts whereas the fifth harmonic rejection is spread between 60-70 dB. This is due to the difference in the systematic HR for the two harmonics. This design could realize HR ratios in excess of 52 dB for all harmonics by very careful layout. While this technique moved the matching requirement for HR to resistors and capacitors in the low frequency IF section, there can still be sensitivity to mismatches in the rotational switches of the mixer. We believe this will ultimately limit the HR that can be obtained in this topology.

As measurements were done on the entire receiver, the flicker noise contribution due to the mixer could not be isolated from other contributing blocks in the IF chain. For this same reason, the IR performance of the mixer also could not be isolated. However, measurements done on the low frequency spot noise figure did not show dependence on the LO frequency, suggesting that flicker noise was primarily from blocks in the IF chain.

Performance summary of the mixers is presented in the table shown in Fig. 4.13. To the best of our knowledge, this is the first publication that presents higher order HR statistics for a mixer with configurable number of phases. In this work, we have presented mixers with a variable number of

N-Phase mixer with NLO Clock	
CMOS Technology	110 nm
Complex Gain of mixer+IF section	19 dB
DSB NF	11 dB
IIP3	12 dBm
IIP2	75 dBm
HR_3,HR_5,HR_7,HR_9	>52, >54, >55, >52 dB
HR_{N-1}[a]	14 dB
No. of Mixer phases	16, 12, 8 and 6
Vdd (Multi-phase mixer, unity gain buffers, opamp)	2.7 V
Vdd (clock)	1.3 V
Current	10 mA (mixer) 12 mA (ug buffers) 12 mA (opamp) 8 mA (clock generation for N=16 at 1.6 GHz)
Power	102 mW

a HR_{N-1} corresponds to N=6

b HR_{N-1} corresponds to N=4 at LO=820 MHz

Figure 3.26: Performance summary.

phases: 16, 12, 8, and 6 for one technique while rejecting up to the 14^{th} harmonic. Most of the published work is on a 8 phase mixer that rejects only the 3^{rd} and 5^{th} harmonics. A mixer with a configurable number of mixer phases involves considerably more design and layout complexity, than an HRM with a fixed number of mixer phases. Higher current is consumed in the rotational pulse generation for a mixer with variable number of phases due to the parasitic capacitive loading of the unused stages. Also, the configurability of sine/cosine weights in the IF section increases the potential for layout imbalances to degrade systematic HR. Despite this, the mixers described in this paper achieve an HRR in excess of 52 dB for harmonics other than the $(N-1)^{th}$ without any trimming or calibration.

3.14 Conclusions

In this chapter we have we have presented a technique that achieves significantly reduced sensitivity to mismatches in devices operating at high frequencies. This technique is verified by a mixer fabricated in a 110 nm CMOS process. While rejecting up to the first 14 harmonics, this mixer achieves 3^{rd}, 5^{th}, 7^{th} and 9^{th} HR ratios in excess of 52 dB, 54 dB, 55 dB and 52 dB respectively, without any trimming or calibration. We have also discussed key performance parameters for these mixers including gain, NF, IR, IIP2, IIP3, and HR. We have presented key circuit implementation details and discussed measured performance results.

Chapter 4

$2N$-Phase Mixer

4.1 Concept

The concept used in this technique is shown in Fig. 4.1. RF signal is multiplied by differential halves (NLO_p and NLO_n) of the NLO clock. The product of RF with NLO_p is rotated to N IF outputs through rotational switch S_p. Like before, the switch S_p transitions from one IF output to the next only when NLO_p is low or when there is no signal through it (Fig. 4.2) reducing its contribution to gain/phase errors and noise in the RF section of the mixer. Similarly, switch S_n rotates the product of RF with NLO_n to another set of N IF outputs.

The intervals when when NLO_p and NLO_n are high alternate in time. Upon multiplication of NLO_p and NLO_n with RF, $2N$ IF outputs are generated. These $2N$ IF outputs when interleaved have uniformly changing phase (Fig. 4.2). The N IF outputs resulting from multiplication of NLO_p and NLO_n with RF constitute the even ($IF_0, IF_2, \ldots IF_{2N-2}$) and odd ($IF_1, IF_3, ..IF_{2N-1}$) mixer phases. The IF section weights and sums the even IF outputs with weights proportional to even samples of a sine wave sampled $2N$ times, to generate IF_{even}, while IF_{odd} is generated by weighting and summing the odd

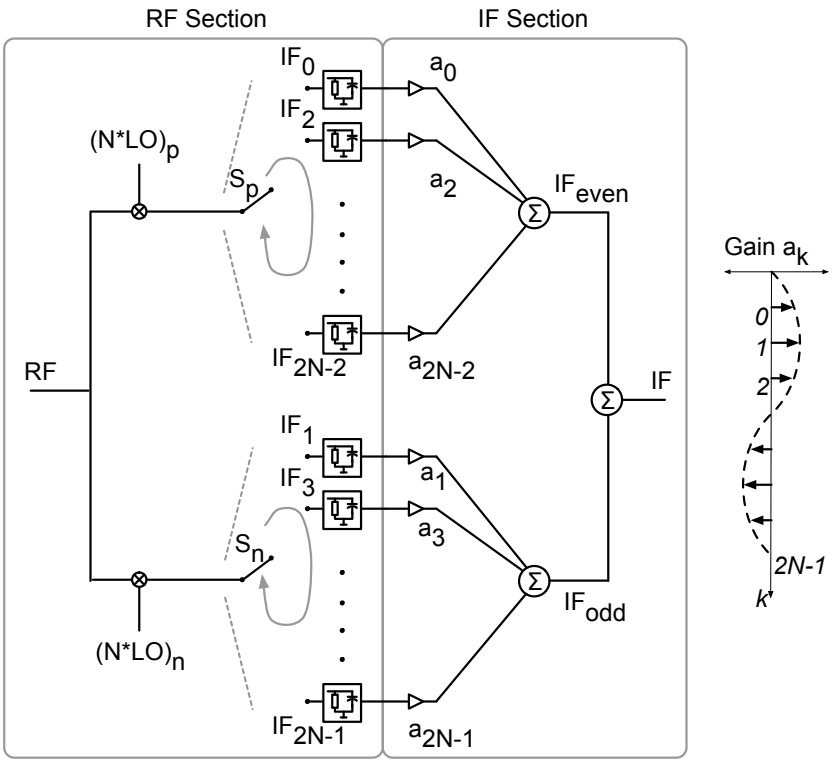


Figure 4.1: Concept of $2N$ phase mixer

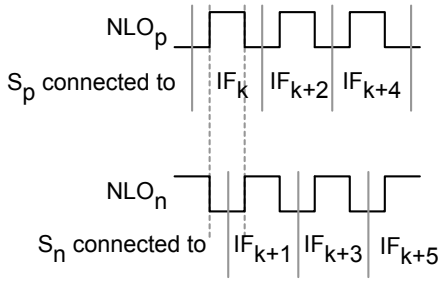


Figure 4.2: Timing of rotation for $2N$ phase mixer.

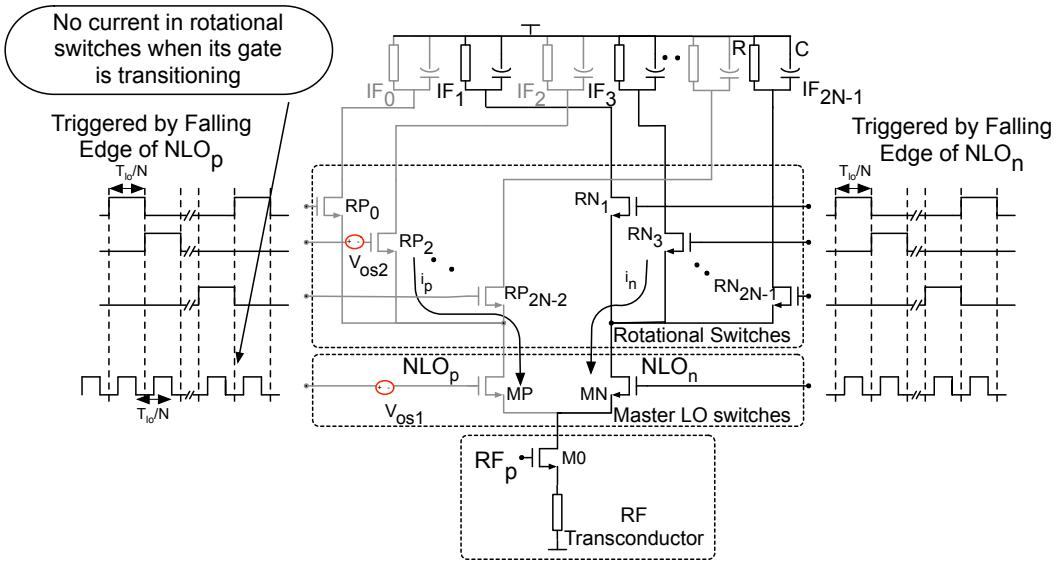


Figure 4.3: RF section of 2N-phase mixer (only single balanced mixer shown for clarity).

IF outputs with the odd samples of a sine wave. For a M-phase HRM, the first un-rejected harmonic is at $M-1$. Therefore, at $IF = IF_{even} + IF_{odd}$ all the harmonics till $2N-1$ are rejected. $(N-1)^{th}$ harmonic rejection is thus achieved.

4.2 Circuit Implementation and Operation of RF Section

An implementation of the RF section of the mixer is shown in Fig. 4.3. Here only a single balanced mixer is shown for clarity. At any given time instant, when NLO_p is high, the RF current of the transconductor flows through MP and one of RP_0, RP_2 or RP_{2N-2} into one of the even IF outputs (IF_0, IF_2 or IF_{2N-2}). Similarly, when NLO_n is high RF transconductor current flows

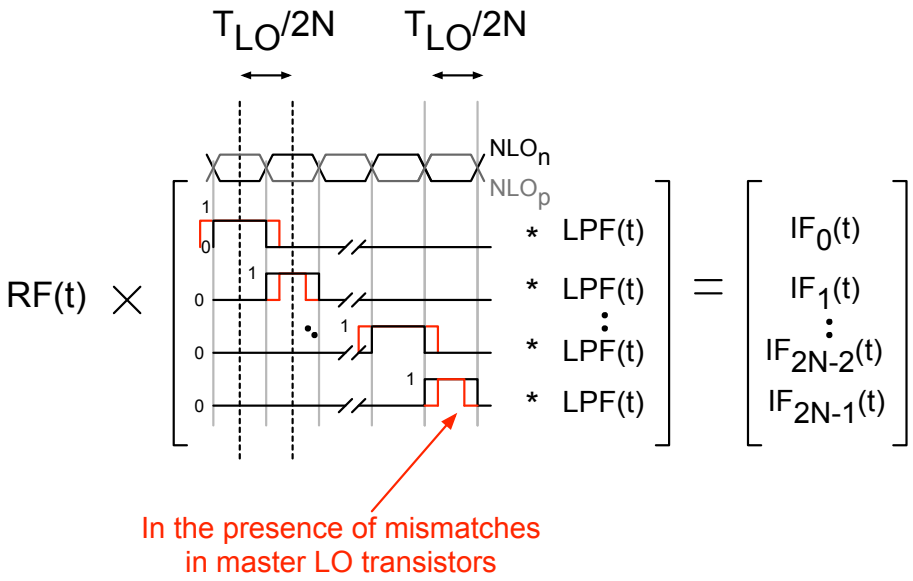


Figure 4.4: RF section functionality.

through MN and one of RN_1, RN_3 or RN_{2N-1} into one of the odd IF outputs (IF_1, IF_3 or IF_{2N-1}).

RP_0-RP_{2N-2} and RN_1-RN_{2N-1} constitute the rotational switches S_p and S_n in Fig. 4.1. The gates of the rotational switches, RP_0-RP_{2N-2} and RN_1-RN_{2N-1}, are driven by $1/N$ duty cycle rectangular waveforms generated from a shift register triggered by the falling edges of NLO_p and NLO_n, respectively. The transitions at the gates of RP_0-RP_{2N-2} and RN_1-RN_{2N-1}, are designed to happen when they carry no current. As each of $RP_0, RN_0, ...RN_{2N-1}$ serially receive their gating pulses, the RF transconductor current gets rotated to the $2N$ IF outputs, $IF_0 - IF_{2N-1}$.

Thus, the operation of this rotational arrangement is equivalent to multiplying the RF current by $1/2N$ duty cycle rectangular waveforms that are

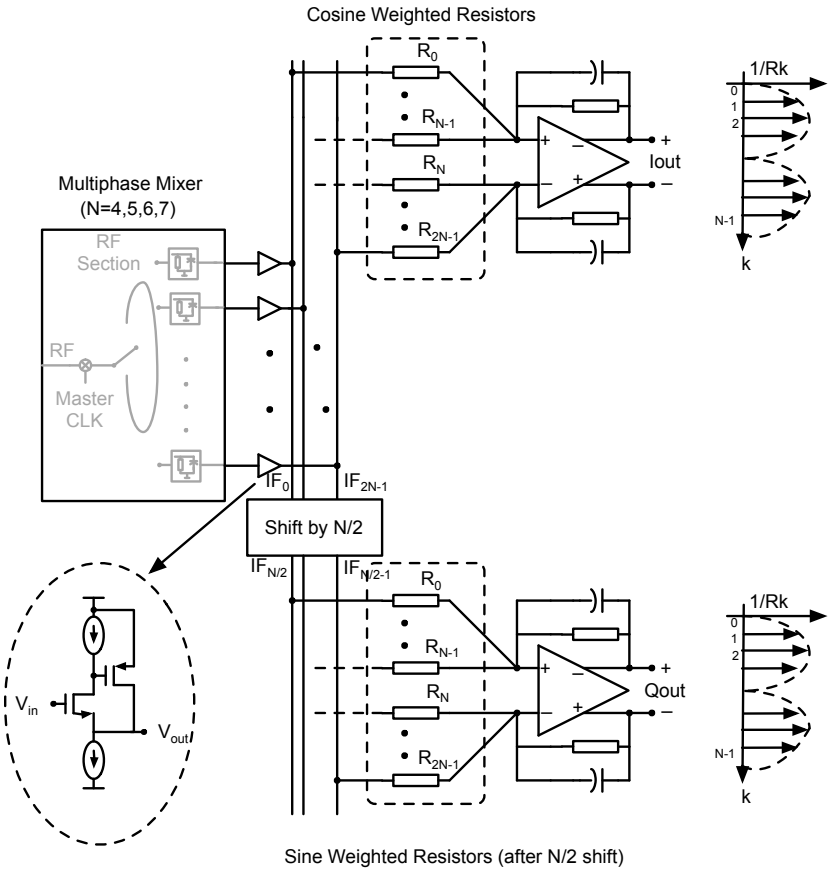


Figure 4.5: Circuit of IF section.

time-shifted as shown in Fig. 4.4. Shunt capacitors (C) in parallel with load resistors (R) provide the low-pass filtering needed for the mixer in Fig. 4.3.

4.3 IF Section Implementation

The implementation of the IF section is shown in 4.5. Here also $2N$ multi-phase mixer outputs are buffered through super source-followers and

2N	Half sine weights	Half cosine weights
8	[0 17 24 17]	[24 17 0 −17]
10	[10.9 21.4 23.75 17 3.75]	[10.9 21.4 23.75 17 3.75]
12	[6.2 17 23.2 23.2 17 6.2]	[23.2 17 6.2 −6.2 −17 −23.2]
14	[2.67 12.75 20.33 23.83 22.67 17 7.9]	[2.67 12.75 20.33 23.83 22.67 17 7.9]

Table 4.1: Sine/Cosine Weights.

weighted with $2N$ samples of Cosine and Sine wave and summed to generate I and Q outputs respectively. In this design, N is programmable to have values of 4, 5, 6 or 7. Hence, this mixer has 8, 10, 12 or 14 mixer phases.

The sine/cosine weights used in this design are shown in Table 4.1. As before, the sine weights are implemented as conductances ($1/R_k$ in Fig. 4.5). The integer part represents the number of unit resistors in parallel while the fractional part is realized using series/parallel combinations of the same unit resistor.

4.4 Non idealities: Mismatches

In the presence of a differential mismatch in the master LO transistors, MP-MN, (represented by V_{os1} in Fig. 4.3), the pulse widths of the currents flowing through them is affected. If S is the differential slope at the zero crossing of the waveform, $NLO_p - NLO_n$, the time that $i_p - i_n$ is positive is increased by $2\Delta t = 2V_{os1}/S$, whereas the time that it is negative reduces by

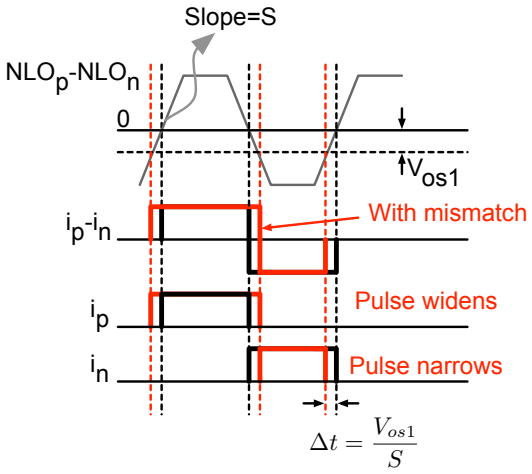


Figure 4.6: Impact of mismatches in NLO clock

the same amount (Fig. 4.6). Another observation is that i_p's (or i_n's) pulse width increases (or decreases) equally on both sides compared to the ideal waveforms. Therefore, the duration between their centers remains unchanged.

Since i_p flows to the even IF outputs and i_n flows to the odd IF outputs, the time of conduction of RF current to even IF outputs differs from the time of conduction to the odd IF outputs. This has an impact on the conversion gains for all frequency translations in the mixing operation (Fig. 4.4). If G_p represents the conversion gain of the p^{th} harmonic component of the rectangular multiplying waveforms shown in Fig. 4.4, then in the presence of mismatches:

$$G_{p-odd} = G_{p-ideal}\,(1 - \epsilon_p) \tag{4.1}$$

$$G_{p-even} = G_{p-ideal}\,(1 + \epsilon_p) \tag{4.2}$$

While the error (ϵ_p) is a function of the harmonic component (p) that is causing the frequency translation, it is proportional to Δt. Thus, mismatches in the master LO transistors cause the conversion gains to the odd and even IF outputs to differ with respect to each other for all frequency translations.

Further as discussed earlier, while the duty cycles of odd/even multiplying waveforms is affected by mismatches, the time duration between the centers of the multiplying waveforms is not. This time duration equals $\frac{T_{LO}}{2N}$ irrespective of the mismatch. Therefore, if $\angle IF_{p,k}$ represents the phase of the signal at IF_k down-converted by the p^{th} harmonic of the rectangular multiplying waveform, then phase relationship between adjacent IF output is the same as in the ideal case and independent of mismatches in the master LO transistors, as shown in (4.3).

$$\angle IF_{p,k+1} - \angle IF_{p,k} = p \cdot \frac{2\pi}{2N} \tag{4.3}$$

While the above analysis focused on the mismatch between the master LO transistors, the conclusions reached can just as well be applied to mismatches in the drivers of the NLO_p/NLO_n clock that affect its differential duty cycle.

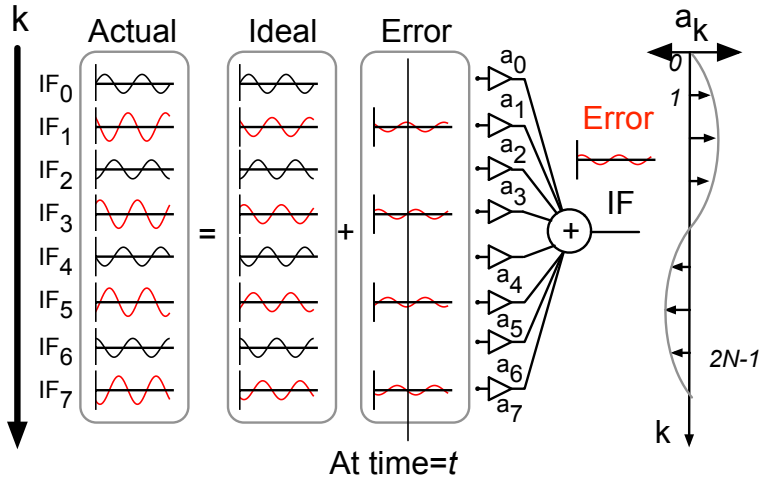
Transitions at the gates of the rotational switches in Fig. 4.3 are designed to happen when there is no current through them. Hence, gates of the

rotational transistors are set-up to the right voltage prior to conduction and at the time of conduction merely serve as cascodes. Edges of the current flowing into any IF output are determined by the edges in the NLO clock. Thus, the mismatches in the rotational switches do not cause any significant gain/phase errors.

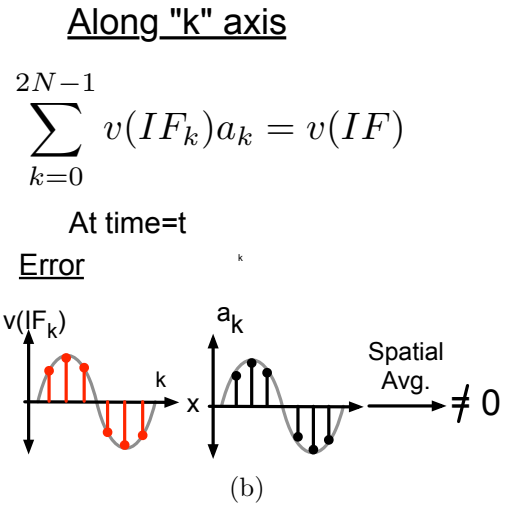
4.5 Impact of Mismatches on HR Performance

Fig. 4.7a shows the down-converted signals in the HRM for the case of $N = 4$, when a tone at a frequency of $(N-1)LO+IF$ is applied at the RF input of the mixer. This tone gets down-converted by the $(N-1)^{th}$ harmonic of the multi-phase LO and appears at a frequency of IF in the outputs $IF_0 - IF_{N-1}$. From (4.3), the phase shift between adjacent IF outputs equals $(N-1)\frac{2\pi}{2N}$. As was discussed earlier, device mismatches in the master LO switching pair (MP-MN in Fig. 4.3) cause gain errors between the odd and even IF outputs, but no phase error. The actual waveforms existing in $IF_0 - IF_{N-1}$ can be split into ideal waveforms (in the absence of device mismatches) and error waveforms (caused by device mismatches). Since the error only exists in the odd (or even) IF outputs, the phase shift between adjacent error waveforms is twice as much as the phase shift between adjacent IF outputs. This equals $2\pi/N$ in absolute value.

Looking along the k axis in Fig. 4.7b at time t, the samples of the error waveforms, complete one period from $k = 0$ to $k = 2N - 1$. This is due to the fact that the phase shift between adjacent error waveforms is

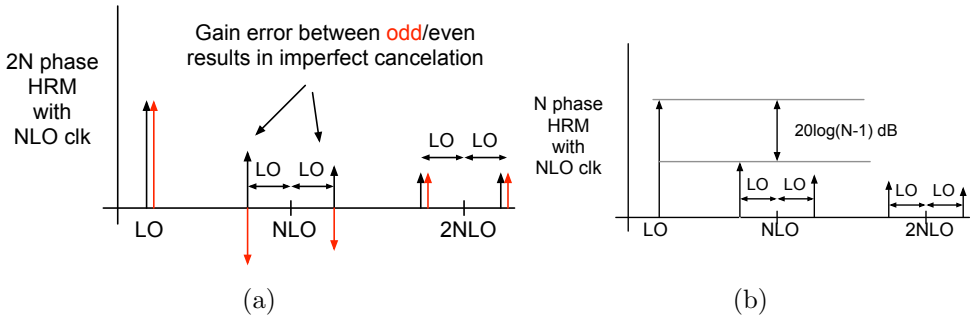


(a)



(b)

Figure 4.7: Impact of mismatches in master LO transistors on HR performance.



(a) (b)

Figure 4.8: LO_{eff} spectrums for (a) 2N-phase HRM and (b) N-phase HRM with NLO clock.

$2\pi/N$ while there are N error waveforms. The error signals are weighted by values proportional to the odd samples of a sine wave sampled $2N$ times. This weighting operation followed by summation can be thought of as multiplication followed by summation. But since two sine waves of the same frequency are not orthogonal, the error does not go to zero after summation. In other words, HR_{N-1} is proportional to the odd/even gain error for this HRM.

The reasoning presented above can be extended to the general case of HR_p, where $1 < p < 2N - 1$ and $p \neq N \pm 1$. In this case, when a signal at a frequency of $pLO + IF$ is present at the RF input of the mixer, it is down-converted by the p^{th} LO harmonic. Again, from (4.3) the phase shift between adjacent IF outputs is $p\frac{2\pi}{2N}$. This results in the phase shift between adjacent error waveforms being $p\frac{2\pi}{N}$. Again looking along the k axis, the samples of the error signal at any given time t, lie on a sine wave that completes p periods along the k axis. But for this case, the samples of the error signal and the sine weighted gains lie on sine waves of different frequencies which are orthogonal.

Thus, the error averages to zero after the sine weighted sum. In summary, the mismatches in the master LO switching pair do not affect the rejection at harmonics other than $p = N \pm 1$.

The effective LO spectrum for the 2N-phase HRM is shown in Fig. 4.8a. The gain error between the odd/even IF outputs results in imperfect cancellation of the $(N \pm 1)^{th}$ LO harmonics, but still provides an improvement over the $(N \pm 1)^{th}$ HR for the N-phase mixer (shown in Fig. 4.8b)

4.6 Flicker Noise Cancellation and IIP2 Performance

While the HRM presented in Chapter 3, canceled flicker noise at the single ended IF output, this HRM achieves flicker noise cancellation after the sine weighted sum.

Flicker noise of the master LO switching devices, can be viewed as a slowly varying voltage source in series with the gates of master LO transistors [23] (V_{os1}) in Fig. 4.3. Depending on the instantaneous value of the noise, transistor MP (in Fig. 4.3) conducts for a longer or shorter duration of time. The opposite is true for transistor MN. Thus, flicker noise modulates the pulse-widths of current through MP and MN. If the pulse-width of current through MP gets wider, then the pulse-width of current through MN gets narrower by an equal amount. The current through MP is rotated to the even IF outputs and the current through MN is rotated to the odd IF outputs. The low pass filter formed by mixer's load R and C (Fig. 4.3) averages the current flowing into any of $IF_0 - IF_{2N-1}$. Thus, the differences in pulse-widths of currents

flowing into odd and even IF outputs gets converted to different average voltages to appear on the odd and even IF outputs. After the effect of the low pass filter, if flicker noise at any IF output at IF_k can be written as $v_{nk}(t)$, then the flicker noise after the sine weighted sum, $v_{n-out}(t)$, can be written as

$$v_{n-out}(t) = \sum_{k=0}^{2N-1} v_{nk}(t) \cdot a_k \tag{4.4}$$

$$v_{n-out}(t) = \sum_{k=even} v_{nk}(t) \cdot a_k + \sum_{k=odd} v_{nk}(t) \cdot a_k \tag{4.5}$$

where $a_k = sin\left(\frac{2\pi k}{2N}\right)$. Given that flicker noise is slowly varying with time, the noise $v_{nk}(t)$ for all odd k is highly correlated and so is $v_{nk}(t)$ for all even k. Hence, we can rewrite above equation as

$$v_{n-out}(t) = v_{n-even}(t) \cdot \sum_{k=even} a_k + v_{n-odd}(t) \cdot \sum_{k=odd} a_k \tag{4.6}$$

But since for a uniformly sampled sine wave $\sum_{k=even} a_k = 0$ and $\sum_{k=odd} a_k = 0$, flicker noise is canceled at the output.

Similar to the effect of flicker noise, mismatches in master LO transistors alter the time of conduction to odd and even IF outputs. As discussed in section III 4.4, conversion gain to the odd and even IF outputs is different in the presence of mismatches in master LO transistors. Considering only the single balanced mixer shown in Fig. 4.3, the IM2 component present in the

RF transconductor's current appears with different gains to the odd and even IF outputs ($p = 0$ in (4.1) and (4.2)) and without any frequency translation. Thus, if $v_{im2-even}(t)$ and $v_{im2-odd}(t)$ are the voltages developed by the IM2 component at even and odd IF outputs respectively, then the IM2 component after the sine weighted sum, $v_{n-out}(t)$, goes to zero, since $\sum_{k=even} a_k = 0$ and $\sum_{k=odd} a_k = 0$ according to the equation below.

$$v_{n-out}(t) = v_{im2-even}(t) \cdot \sum_{k=even} a_k + v_{im2-odd}(t) \cdot \sum_{k=odd} a_k \tag{4.7}$$

Here again, mismatches in the rotational switches are not significant as they merely act as cascodes. Hence, the IIP2 performance is limited by resistor/capacitor matching in the IF section. By using large resistor areas, superior IIP2 performance is achieved.

4.7 Measurements and Discussion

The 2N-phase HRM presented is fabricated in 55 nm standard CMOS process as part of a receiver (Fig. 4.9). The same RF mixer core can be configured differently for $N = 4$, 5, 6 or 7 to produce 8, 10, 12 and 14 phases, respectively. Multi-phase mixer and unity gain buffers draw 10 mA and 12 mA respectively from 2.8 V regulated supply. Multi-phase rotational pulse generation and master clock buffering consumes 19 mA from 1.3 V with a master clock of 4 GHz in the $N = 4$ mode. Extrapolated from the receiver measurements, the IIP3 and DSB NF of the mixer are 12 dBm and 12 dB

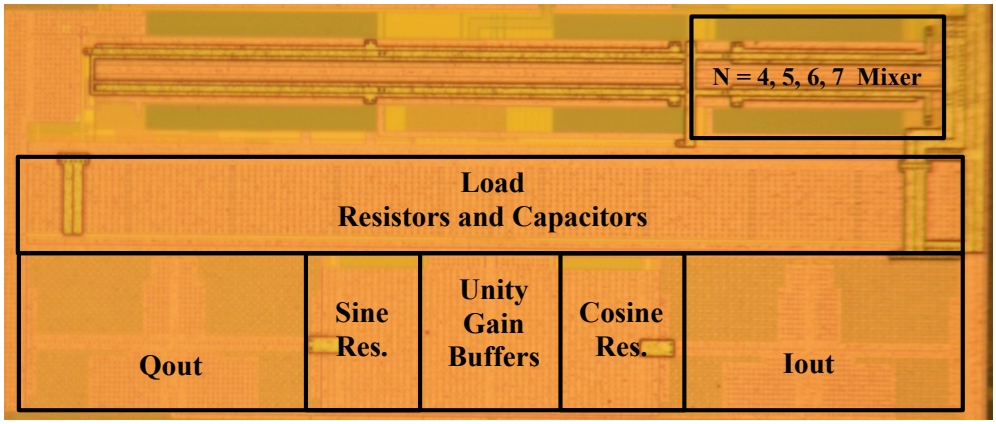
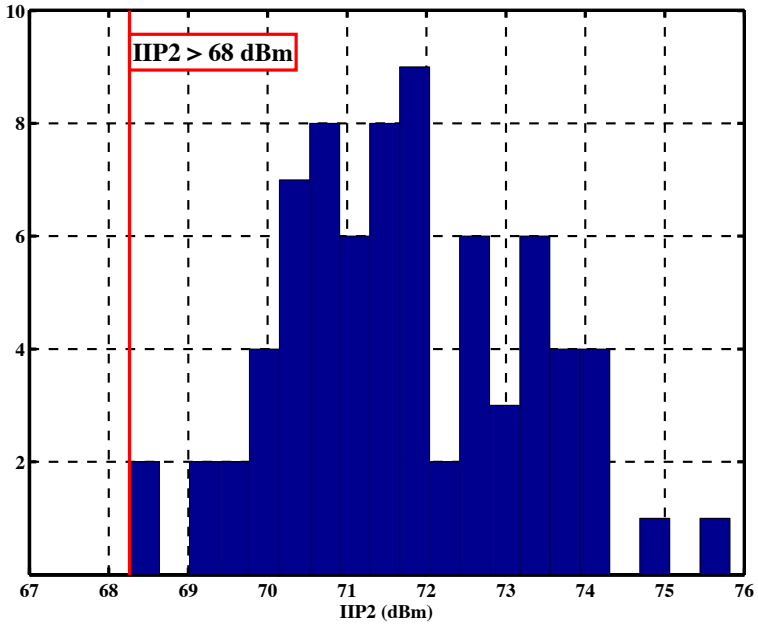


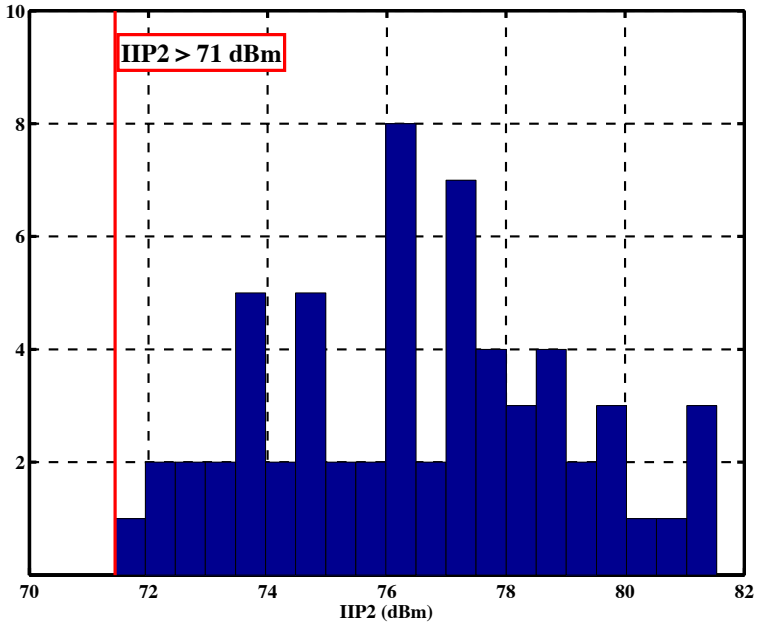
Figure 4.9: Die Photo of 2N-phase HRM with NLO Clock.

respectively. The multi-phase mixer load resistors occupy 0.008 mm^2 and the sine/cosine-weighted resistors with switches, 0.028 mm^2.

Fig. 4.12a shows the measured 3^{rd} HR ratio for 150 parts for $N = 4$, 5, 6 and 7. The desired channel frequencies were 820 MHz, 800 MHz, 632 MHz and 472 MHz for $N = 4$, 5, 6 and 7 respectively. For this measurement, interferers were applied at both 3LO+IF and 3LO-IF and rejection was measured at both these frequency points. The worse of the rejection between these two measurements is shown in the Fig. 4.12a. The 3^{rd} HR ratio for $N = 5$, 6 and 7 is in excess of 52 dB. This is due to the fact that the mixer's 3^{rd} HR for these frequencies is determined by device matching at IF frequencies. For $N = 4$, the 3^{rd} HR ratio is in excess of 39 dB measured over 150 parts. For the mixer presented in Section 3, the $(N-1)^{th}$ harmonic rejection is only $20log(N-1)$ dB. For $N = 4$, this is only 10 dB. Compared to this case, the technique presented here achieves an enhancement of about 29 dB. The dominant source



(a) IIP2 for N=4 at RF=862 MHz



(b) IIP2 for N=5 at RF=682 MHz

Figure 4.10: IIP2 Histograms for N=4 and N=5

Harmonic Rejection Summary (>150 samples)					
N	LO Frequency	Clock Frequency	First Unrejected Harmonic Frequency	HR3	HR4
4	820 MHz	3.28 GHz	5.74 GHz	>39dB	>52dB
5	800 MHz	4.00 GHz	7.20 GHz	>52dB	>41dB
6	682 MHz	4.09 GHz	7.5 GHz	>52dB	>52dB
7	472 MHz	3.30 GHz	6.13 GHz	>52dB	>52dB

Figure 4.11: Tabular Summary of HR performance of 2N-phase HRM with NLO Clock.

of finite 3^{rd} HR for $N = 4$ are the duty cycle errors in the differential NLO clock. These duty cycle errors arise due to mismatches in devices operating at RF frequencies. There is a 12 dB difference between the 3^{rd} HR ratio for $N =$ 5, 6 and 7 (whose HR was determined by IF matching) and for $N = 4$. This validates the advantage of matching devices in the IF circuits rather than in the RF part, for achieving higher HR performance.

Fig. 4.12b shows the 4^{th} HR measurements for $N = 4$, 5, 6 and 7. Minimum of the 4^{th} HR ratio for $N = 5$ is 41 dB whereas, for $N = 4$, 6 and 7, the 4^{th} HR ratio is in excess of 54 dB. This again is consistent with the theoretical expectations from section III4.5 that $(N-1)^{th}$ harmonic should have worse rejection as the $(N-1)^{th}$ HR is determined by RF matching. The 4^{th} HR ratio for all other N is much better. The results are summarized in

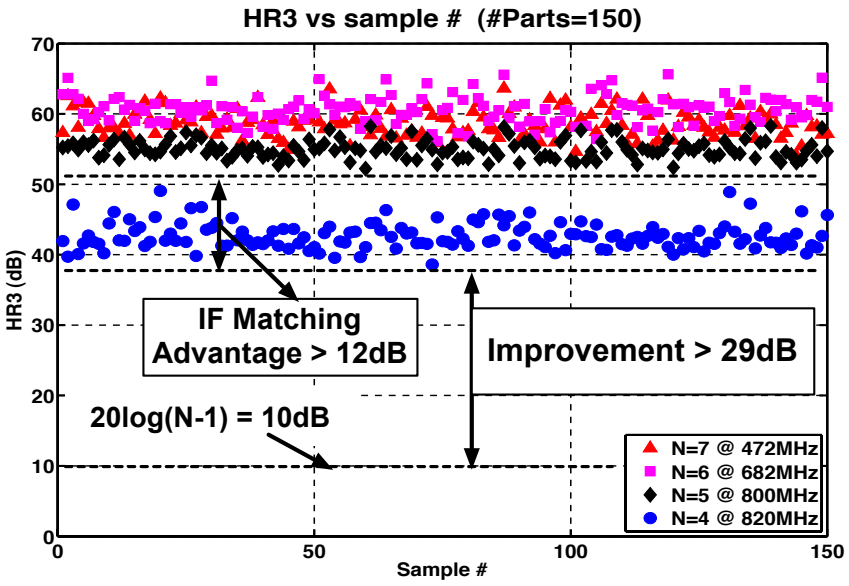
the table shown in Fig. 4.11.

The measured IIP2 performance of the mixer extrapolated from measurements done on the receiver is shown in Fig. 4.10. IIP2 was measured using Automatic Test Equipment. For N=5 and at an RF frequency of 682MHz, the measured IIP2 over 75 parts is better than 71 dBm. For N=4 and at an RF frequency of 862 MHz, the measured IIP2 of over 60 parts is better than 68 dBm. We believe this difference is due to layout as the configuration of the IF section and the RF section of the mixer is different for these two value of N.

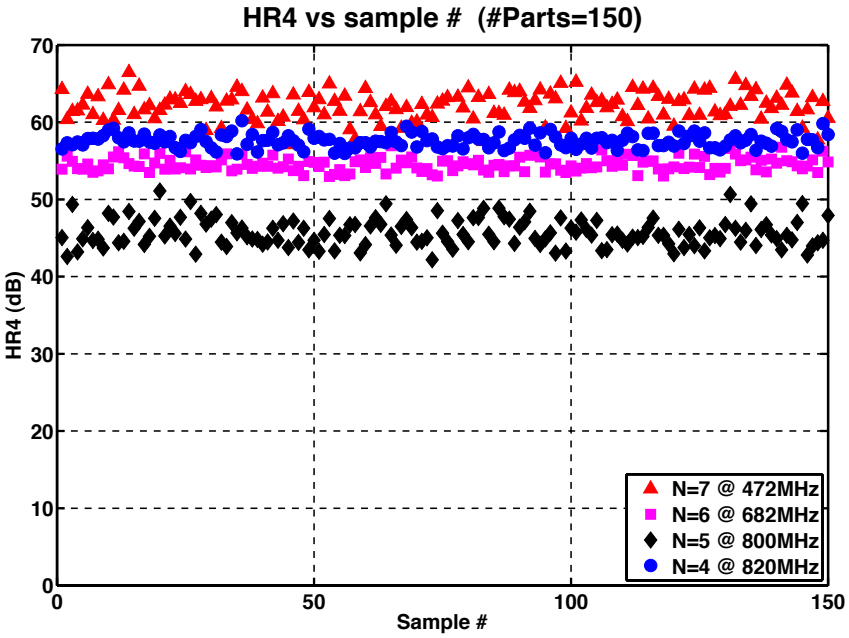
Performance summary of the mixers is presented in the table shown in Fig. 4.13. A mixer with a configurable number of mixer phases involves considerably more design and layout complexity, than an HRM with a fixed number of mixer phases. Higher current is consumed in the rotational pulse generation for a mixer with variable number of phases due to the parasitic capacitive loading of the unused stages. Also, the configurability of sine/cosine weights in the IF section increases the potential for layout imbalances to degrade systematic HR. Despite this, the mixers described in this paper achieve an HRR in excess of 52 dB for harmonics other than the $(N-1)^{th}$ without any trimming or calibration.

4.8 Conclusions

In this chapter we have described a technique to achieve additional rejection of the previously un-rejected $(N-1)^{th}$ LO harmonic while preserving



(a)



(b)

Figure 4.12: Measured HR3 and HR4 for N=4,5,6,7.

2N-Phase mixer with NLO Clock	
CMOS Technology	55 nm
Complex Gain of Mixer + IF section	19 dB
DSB NF	12 dB
IIP3	12 dBm
IIP2	>68 dBm
HR_3	>52 dB
HR_{N-1}[a]	>39 dB
No. of Mixer phases	14, 12, 10 and 8
Vdd (Multi-phase mixer, unity gain buffers, opamp)	2.8 V
Vdd (clock)	1.3 V
Current	10 mA (mixer) 12 mA (ug buffers) 10 mA (opamps) 20 mA (clock generation for N=4 at 4 GHz)
Power	116 mW

[a] HR_{N-1} corresponds to N=4 at LO=820 MHz

Figure 4.13: Performance summary.

the level of rejection for other harmonics. We have verified this technique by a mixer fabricated in a 55 nm CMOS process. This mixer has a programmable number of 8, 10, 12 or 14 mixer phases and achieves an improvement of 29 dB for the $(N-1)^{th}$ LO harmonic while achieving 52 dB of rejection for the 3^{rd} harmonic. We have discussed the key differences in performance parameters with respect to the mixer described in the earlier chapter. We have presented key circuit implementation details and discussed measured performance results.

Chapter 5

Conclusions

5.1 Summary

This dissertation addresses the key challenges in the design of a low-cost wideband receiver. For a wideband system like television with a large input frequency range (48-860 MHz), the problem of LO harmonic rejection is an important one. The achievement of high level of rejection for all LO harmonics translates to reduced pre-mixer RF filtering and low-cost solutions. We have presented two HR mixing techniques using 1) An N-phase HRM using a NLO clock and 2) A 2N phase HRM using a NLO clock. These techniques realize a higher level of rejection for all relevant harmonics.

5.2 Original Contributions

- A generalized $N-$phase HR mixing technique is proposed that has significantly reduced sensitivity to mismatches in devices operating at high frequencies. Conversions gains and relative phase for all frequency translations associated with this mixing operation have this reduced sensitivity. As a consequence, this technique achieves superior HR, IIP2 and IR performance. This active HRM also rejects the flicker noise of the

transistors in the switching pair. This technique is verified by measured results on silicon fabricated in 110 nm CMOS process.

- The above technique rejects the (N-1)th harmonic only by an amount of $20log(N-1)$ dB. A new HR mixing technique is presented that achieves additional rejection of the previously un-rejected $(N-1)^{th}$ harmonic while preserving the level of rejection for the other harmonics. This technique is verified by measurements done on silicon fabricated in 55 nm CMOS process.

- While the published literature has focused only on a 8-phase mixer and the rejection of the 3rd and 5th LO harmonics, this work achieves higher HR performance on higher order harmonics as well. In this work, we have presented a configurable 16,12,8 and 6 phase HRM rejecting up to the first 14 harmonics using the first technique and a mixer with configurable 14, 12 10 and 8 rejecting up to the first 12 harmonics using the second technique. A mixer with a configurable number of mixer phases involves considerably more design and layout complexity, than an HRM with a fixed number of mixer phases. Despite this, the mixers described in this work achieve HR ratios in excess of 52 dB for harmonics other than the $(N-1)^{th}$ without any trimming or calibration.

- A theoretical analysis of the key performance parameters of gain, NF, IIP3, IIP2 and HR for the new HR mixer topologies is presented.

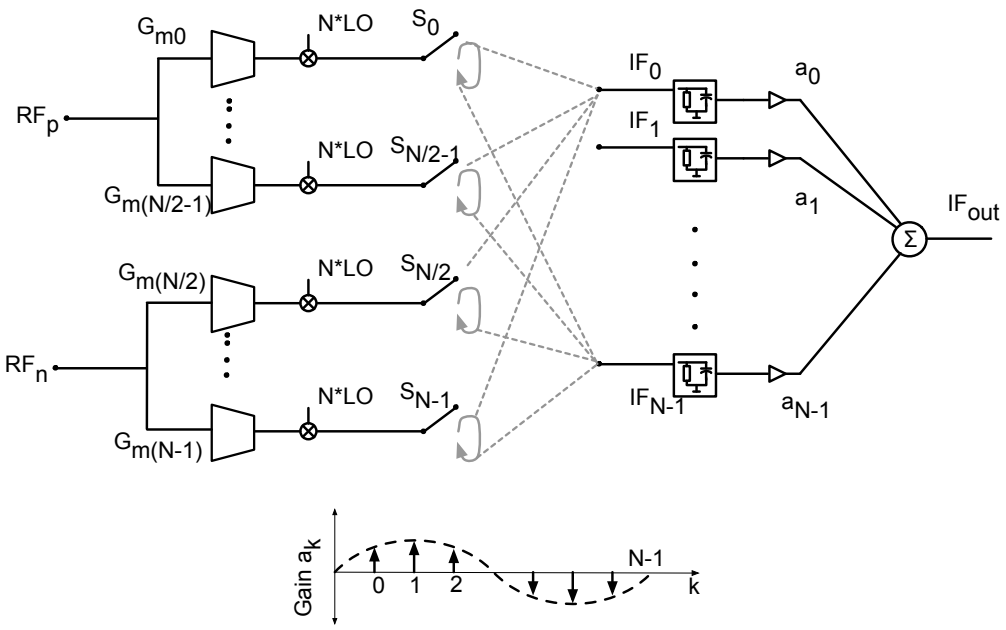


Figure 5.1: 2-Stage Clock-Gated HRM

5.3 Suggestions for Future Work

5.3.1 2-Stage Clock-Gated HRM

While the technique presented in [6] is limited by phase errors in achieving a higher HR performance, the clock-gated mixing techniques presented in this dissertation do not suffer from such impairment. A further enhancement in HR performance can be achieved by using the clock-gated mixer in a 2-stage configuration. As shown in Fig. 5.1, RF sections of N, N-phase mixers are interleaved. The RF transconductor of each N-phase mixer is sine weighted as per (5.1).

$$G_{mk} \propto \mid sin(\left(\frac{2\pi k}{N}\right) \mid \tag{5.1}$$

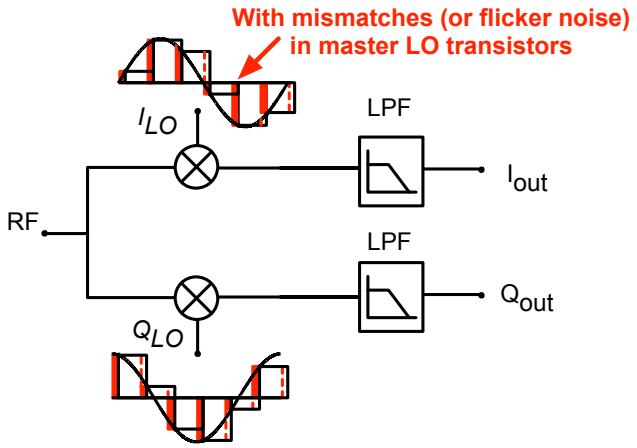


Figure 5.2: A simplified equivalent model for the mixer.

At any given time, the switches $S_0 \ldots S_{N-1}$ provide a conducting path to N distinct IF outputs ($IF_0 - IF_{N-1}$). In other words, two switches do not connect to the same IF output at the same instant. The rotation of the RF signal occurs as follows: If at time t switches S_0, S_1, $\ldots S_{N-1}$ provide a conductive path to IF_k, IF_{k+1}, $\ldots IF_{N-1+k}$ respectively, then at time $t + \frac{T_{LO}}{N}$ switches S_0, S_1, $\ldots S_{N-1}$ connect to IF_{k+1}, IF_{k+2}, $\ldots IF_{N+k}$. The sine weighted RF transconductor current is thus rotated to N IF outputs. As before, the rotation happens when the switches carry no instantaneous current. This results in reduced sensitivity to mismatches in switches and lower phase errors in multi-phase IF generation.

5.3.1.1 HR Benefit

The equivalent model for the N-phase HRM is shown in Fig.5.2. The signal at the RF port of the mixer is equivalently multiplied by staircase ap-

proximations to sine/cosine waves, $I_{LO}(t) + jQ_{LO}(t)$, and low-pass filtered to generate quadrature outputs. Here we will use this model for each of the N, N-phase HRMs to illustrate the HR benefit in the 2 stage HRM. $+v_{RF}(t)/2$ and $-v_{RF}(t)/2$ are the input signals at RF_p and RF_n in Fig. 5.1. Using the equivalent model, the current at the outputs of each transconductor, G_{mk}, is multiplied by an effective complex LO ($I_{LO_k}(t) + jQ_{LO_k}(t)$) and low-pass filtered by the mixer's load RC. Ideally, $I_{LO}(t)+jQ_{LO}(t)$, has no harmonics other than at $mN\pm1$. But in the presence of mismatches in the IF section that cause deviations in the sine/cosine weights, $I_{LO}(t) + jQ_{LO}(t)$ has harmonic content. In the analysis that follows, let us assume that $I_{LO}(t)+jQ_{LO}(t)$ represents the practical case and has finite harmonic rejection. Even with the mismatches in the IF sections, $I_{LO_{k+1}}(t) + jQ_{LO_{k+1}}(t)$ is identical to$I_{LO_k}(t) + jQ_{LO_k}(t)$ in shape but is shifted in time. This is because both $I_{LO_k}(t) + jQ_{LO_k}(t)$, and $I_{LO_{k+1}}(t) + jQ_{LO_{k+1}}(t)$ are generated from the same IF section weights. The time shift is $\frac{T_{LO}}{N}$ but in the presence of mismatches in the NLO switching pair, it deviates from this value as described in Chapter 3. For each of the N, N-phase HRMs the mismatches in the NLO switching pair are un-correlated. Thus, Δ_k in the equation below are independent random variables.

$$I_{LO_k}(t) + jQ_{LO_k}(t) = I_{LO_0}(t - \frac{kT_{LO}}{N} - \Delta_k) + jQ_{LO_0}(t - \frac{kT_{LO}}{N} - \Delta_k) \quad (5.2)$$

Taking the Fourier transform on both sides, we have

$$I_{LO_k}(f) + jQ_{LO_k}(f) = \{I_{LO_0}(f) + jQ_{LO_0}(f)\} \cdot exp\left\{-j2\pi f\left(\frac{kT_{LO}}{N} + \Delta_k\right)\right\} \tag{5.3}$$

Thus, the signal at the output can be written as follows:

$$I_{out}(t) + jQ_{out}(t) = \frac{v_{RF}(t)}{2}\left[\sum_{k=0}^{N-1} G_{mk}\left(I_{LO_k}(t) + jQ_{LO_k}(t)\right)\right] \otimes LPF(t) \tag{5.4}$$

where LPF(t) is the impulse response of the low pass filter formed at the mixer's output due to R and C, and $\otimes$represents convolution. Taking the Fourier transform on both sides, gives us

$$I_{out}(f) + jQ_{out}(f) = \frac{V_{RF}(f)}{2} \otimes \left[\sum_{k=0}^{N-1} G_{mk}\left(I_{LO_k}(f) + jQ_{LO_k}(f)\right)\right] \cdot LPF(f) \tag{5.5}$$

Using (5.3) in (5.5) gives us

$$I_{out}(f) + jQ_{out}(f) = \frac{V_{RF}(f)}{2} \otimes \left[\left(I_{LO_0}(f) + jQ_{LO_0}(f)\right) \sum_{k=0}^{N-1} G_{mk} \cdot exp\left\{-j2\pi f\left(\frac{kT_{LO}}{N} + \Delta_k\right)\right\}\right] \cdot LPF(f) \tag{5.6}$$

The term in square paranethesis is composed of the product of two terms: 1) $I_{LO_0}(f) + jQ_{LO_0}(f)$ and 2) $\sum_{k=0}^{N-1} G_{mk} \cdot exp\left\{-j2\pi f\left(\frac{kT_{LO}}{N} + \Delta_k\right)\right\}$. Thus, the spectrum of $I_{LO_0}(f)+jQ_{LO_0}(f)$ gets shaped further by the frequency response of the second term. If the harmonic rejection in the first term was x dB, and the attenuation at the harmonic frequency due to the second term term was y dB, then the total harmonic rejection for this mixing scheme will be $x + y$ dB. The work in this dissertation has proved that it is possible to achieve a rejection in excess of 50 dB for the harmonic in the first term, $I_{LO_0}(f) + jQ_{LO_0}(f)$. The second term is affected by the mismatches in the various sine weighted RF transconductors, G_{mk} and by mismatches in the transistors of the NLO switching pair affecting Δ_k. This is very similar to the conventional HRM sensitive to gain/phase errors caused by mismatches in devices operating at RF frequencies. It s reasonable to expect a rejection at the harmonic frequencies of 30-40 dB from the second term [5, 34]. Thus, this approach of could achieve an effective harmonic rejection in the 80-90 dB range, clearly excelling the current state-of-the-art of 60 dB for the third/fifth harmonic rejection in [6, 62].

This benefit of using the clock-gated mixing scheme presented in this dissertation in a 2-stage configuration arises due to the significantly reduced phase errors in this mixing scheme. Hence, in (5.2), $I_{LO_k}(t) + jQ_{LO_k}(t)$ can simply be written as a time shifted version of $I_{LO_0}(t) + jQ_{LO_0}(t)$ for any k. This will not have been true if there were uncorrelated phase errors in each of $I_{LO_k}(t) + jQ_{LO_k}(t)$.

Bibliography

[1] J.-M. Stevenson, P. Hisayasu, A. Deiss, B. Abesingha, K. Beumer, and J. Esquivel, "A Multi-Standard Analog and Digital TV Tuner for Cable and Terrestrial Applications,," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2007, pp. 210–597.

[2] L. Connell, N. Hollenbeck, M. Bushman, D. McCarthy, S. Bergstedt, R. Cieslak, and J. Caldwell, "A CMOS Broadband Tuner IC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 400–401.

[3] J. van Sinderen, F. Seneschal, E. Stikvoort, F. Mounaim, M. Notten, H. Brekelmans, O. Crand, F. Singh, M. Bernard, V. Fillatre, and A. Tombeur, "A 48-860mhz digital cable tuner ic with integrated rf and if selectivity," in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 2003, pp. 444–506 vol.1.

[4] J. A. Weldon, J. C. Rudell, L. Lin, R. S. Narayanaswami, M. Otsuka2, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. R. Gray, "A 1.75 GHz Highly-Integrated Narrow-band CMOS Transmitter with Harmonic-Rejection Mixers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2001, pp. 160–161, 442.

[5] Z. Ru, E. A. M. Klumperink, and B. Nauta, "A Discrete-Time Mixing Receiver Architecture with Wideband Harmonic Rejection," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2008, pp. 322–616.

[6] Z. Ru, E. A. M. Klumperink, G. J. M. Wienk, and B. Nauta, "A Software-Defined Radio Receiver Architecture robust to Out-Of-Band Interference," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 230–231,231a.

[7] J. Greenberg, F. D. Bernardinis, C. Tinella, A. Milani, J. Pan, P. Uggetti, M. Sosio, S. Dai, S. Tang, G. Cesura, G. Gandolfi, V. Colonna, and R. Castello, "A 40MHz-to-1GHz Fully Integrated Multistandard Silicon Tuner in 80nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 162–163.

[8] N. A. Moseley, E. Klumperink, and B. Nauta, "A Two-Stage Approach to Harmonic Rejection Mixing Using Blind Interference Cancellation," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 10, pp. 966–970, 2008.

[9] N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Experimental verification of a harmonic-rejection mixing concept using blind interference canceling," in *Wireless Technology, 2008. EuWiT 2008. European Conference on*, 2008, pp. 210–213.

[10] N. A. Moseley, Z. Ru, E. A. M. Klumperink, and B. Nauta, "A 400-to-900 MHz Receiver with Dual-Domain Harmonic Rejection exploiting Adaptive Interference Cancellation," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2009, pp. 232–233,233a.

[11] "ATSC Recommended Practice: Receiver Performance Guidelines, ATSC A/74," Advanced Television Systems Committee, Tech. Rep., Jun. 2004.

[12] http://www.etsi.org.

[13] "Mobile and Portable DVB-T/H Radio Access- Part I- Interface Specifications," EICTA, Tech. Rep., 2007.

[14] "Mobile and Portable DVB-T/H Radio Access-Part II- Interface Conformance Testing," EICTA, Tech. Rep., 2008.

[15] C.-H. Heng, M. Gupta, S.-H. Lee, D. Kang, and B.-S. Song, "A CMOS TV tuner/demodulator IC with Digital Image Rejection," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, Feb., pp. 432–608 Vol. 1.

[16] H. Chun-Huat, M. Gupta, L. Sang-Hoon, D. Kang, and S. Bang-Sup, "A CMOS TV tuner/demodulator IC with Digital Image Rejection," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2525–2535, 2005.

[17] "Data-Over-Cable Service Interface Specifications, Radio Frequency Interface Specification, CM-SP-RFIv2.0-C02-090422," Tech. Rep.

[18] "DOCSIS Radio Frequency Interface Specifications-SP-RFIv2.0-I02-020617," Cable Laboratories, Inc. , Tech. Rep., June 2002.

[19] "OpenCable Host Device Core Functional Requirements - OC-SP-HOST-CFR-111-021126," Cable Laboratories, Inc., Tech. Rep., June 2002.

[20] "Digital Cable Network Interface Standard SCTE 40," Soceity of Cable Telecommunications Engineers, Tech. Rep., 2011.

[21] Behzad Razavi, *RF Microelectronics*. Prentice Hall Communications Engineering and Emerging Technologies Series, 2011.

[22] B. Gilbert, "Translinear Circuits: A Proposed Classification," *Electronics Letters*, vol. 11, no. 1, pp. 14–16, 9.

[23] H. Darabi and A. A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," in *IEEE J. Solid-State Circuits*, vol. vol. 35, Jan. 2000., pp. pp. 15–25.

[24] M. T. Terrovitis and R. G. Meyer, "Noise in Current-Commutating CMOS mixers," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 6, pp. –783, 1999.

[25] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz 1/f corner Direct Conversion CMOS receiver," in *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, Sept., pp. 459–462.

[26] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a Direct Conversion Front-end with 3.5-dB NF and 200-kHz 1/f noise corner," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 4, pp. 970–977, April 2005.

[27] A. Mirzaei, H. Darabi, J. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and Optimization of Current-Driven Passive Mixers in Narrowband Direct-Conversion Receivers," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2678–2688, Oct. 2009.

[28] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and Optimization of Direct-Conversion Receivers With 25% Duty-Cycle Current-Driven Passive Mixers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, no. 9, pp. 2353–2366, Sept.

[29] M. Dawkins, A. P. Burdett, and N. Cowley, "A Single-Chip Tuner for DVB-T," in *IEEE J. Solid-State Circuits*, vol. 38, Aug. 2003, pp. 1307–1317.

[30] R. Montemayor, "A 410-mw 1.22-GHz Downconverter in a Dual-Conversion Tuner IC for OpenCable Applications," in *IEEE J. Solid-State Circuits*, vol. 39, Apr. 2004, pp. 714–718,.

[31] S. Lerstaveesin, M. Gupta, D. Kang, and S. Bang-Sup, "A 48-860 MHz CMOS Low-IF Direct-Conversion DTV Tuner," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 9, pp. 2013–2024, 2008.

[32] I. Mak and R. Martins, "A 0.46mm^2 4dB-NF Unified Receiver Front-End for Fullband Mobile TV in 65nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 172–173.

[33] D. Im, H. Kim, and K. Lee, "A Broadband CMOS RF Front-End for Universal Tuners Supporting Multi-Standard Terrestrial and Cable Broadcasts," in *IEEE J. Solid-State Circuits*, vol. 47, Feb. 2012, pp. 392–406.

[34] R. Bagheri, A. Mirzaei, S. Chehrazi, M. Heidari, M. Lee, M. Mikhemar, M. Tang, and A. Abidi, "An 800MHz to 5GHz Software-Defined Radio Receiver in 90nm CMOS," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 1932–1941.

[35] A. A. Rafi, A. Piovaccari, P. Vancorenland, and T. Tuttle, "A Harmonic Rejection Mixer robust to RF Device Mismatches," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2011, pp. 66–68.

[36] A. A. Rafi and T. R. Viswanathan, "Harmonic Rejection Mixing Techniques using Clock Gating," *Solid-State Circuits, IEEE Journal of*, August, 2013.

[37] ——, "Clock-Gated Harmonic Rejection Mixers," in *IEEE Custom Integrated Circuits Conf. (CICC)*, 2012.

[38] J. R. Tourret, S. Amiot, M. Bernard, M. Bouhamame, C. Caron, O. Crand, G. Denise, V. Fillatre, T. Kervaon, M. Kristen, L. Lo Coco, F. Mercier,

J. M. Paris, F. Pichon, S. Prouet, V. Rambeau, S. Robert, J. van Sinderen, and O. Susplugas, "SiP Tuner With Integrated LC Tracking Filter for Both Cable and Terrestrial TV Reception," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 12, pp. 2809–2821, 2007.

[39] S. Sanggyu, R. Kuhn, B. Pflaum, and C. Muschallik, "A Three-band-tuner for Digital Terrestrial and Multistandard reception," *Consumer Electronics, IEEE Transactions on*, vol. 48, no. 3, pp. 709–717, 2002.

[40] S. Sim, R. Kuhn, B. Pflaum, and C. Muschallik, "A Three-band-tuner for Digital Terrestrial and Multistandard reception," in *Consumer Electronics, 2002. ICCE. 2002 Digest of Technical Papers. International Conference on*, 2002, pp. 356–357.

[41] C. Ling, R. Montemayor, A. Cicalini, K. Wang, L. Jansson, L. Mucke, P. Trihka, and S. Y. Kishore, "A Low-power Integrated Tuner for Cable-Telephony Applications," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, vol. 2, 2002, pp. 264–500.

[42] C. Ling, R. Montemayor, A. Cicalini, K. Wang, L. Jansson, L. Mucke, P. Trihka, and S. V. Kishore, "A Low-power Integrated Tuner for Cable Telephony Applications," *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 12, pp. 1757–1767, 2002.

[43] I. Mehr, S. Rose, S. Nesterenko, D. Paterson, R. Schreier, H. L'Bahy, S. Kidambi, M. Elliott, and S. Puckett, "A Dual-Conversion Tuner for

Multi-standard Terrestrial and Cable reception," in *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, 2005, pp. 340–343.

[44] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS Mixers and Polyphase Filters for Large Image Rejection," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 6, pp. 873–887, 2007.

[45] M. Gupta, S. Lerstaveesin, D. Kang, and B. S. Song, "A 48-to-860MHz CMOS Direct-Conversion TV Tuner," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 206–597.

[46] K. Muhammad, D. Leipold, B. Staszewski, Y.-C. Ho, C. Hung, K. Maggio, C. Fernando, T. Jung, J. Wallberg, J.-S. Koh, S. John, I. Deng, O. Moreira, R. Staszewski, R. Katz, and O. Friedman, "A discrete-time bluetooth receiver in a 0.13 mu;m digital cmos process," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, Feb., pp. 268–527 Vol.1.

[47] D. Jakonis, K. Folkesson, J. Dbrowski, P. Eriksson, and C. Svensson, "A 2.4-GHz RF sampling receiver front-end in 0.18- μm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 6, pp. 1265–1277, June.

[48] Z. Ru, E. A. M. Klumperink, and B. Nauta, "On the Suitability of Discrete-Time Receivers for Software-Defined Radio," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, May, pp. 2522–2525.

[49] H.-K. Cha, S.-S. Song, H.-T. Kim, and K. Lee, "A CMOS Harmonic Rejection Mixer With Mismatch Calibration Circuitry for Digital TV Tuner Applications," in *Microwave and Wireless Components Letters, IEEE*, vol. 18, no. 9, 2008, pp. 617–619.

[50] Yannis Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd ed. WCB/McGraw Hill, 1999.

[51] A. Abidi, "High-Frequency Noise Measurements on FET's with Small Dimensions," *Electron Devices, IEEE Transactions on*, vol. 33, no. 11, pp. 1801 – 1805, nov 1986.

[52] P. Klein, "An Analytical Thermal Noise Model of Deep Submicron MOSFET's for Circuit Simulation with Emphasis on the BSIM3v3 SPICE Model," in *Solid-State Device Research Conference, 1998. Proceeding of the 28th European*, sept. 1998, pp. 460 –463.

[53] M. Deen, C.-H. Chen, and Y. Cheng, "MOSFET Modeling for Low Noise RF Circuit Design," in *Custom Integrated Circuits Conference, 2002. Proceedings of the IEEE 2002*, may 2002, pp. 201 –208.

[54] A. Scholten, L. Tiemeijer, R. van Langevelde, R. Havens, A. Zegers-van Duijnhoven, and V. Venezia, "Noise Modeling for RF CMOS Circuit Simulation," *Electron Devices, IEEE Transactions on*, vol. 50, no. 3, pp. 618 – 632, march 2003.

[55] Simon Haykin and Michael Moher, *Communication Systems*, 5th ed. John Wiley and Sons, 2009.

[56] H. Darabi and J. Chiu, "A Noise Cancellation Technique in Active RF-CMOS Mixers," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 12, pp. 2628–2632, 2005.

[57] R. S. Pullela, T. Sowlati, and D. Rozenblit, "Low Flicker-Noise Quadrature Mixer Topology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2006, pp. 1870–1879.

[58] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order Intermodulation Mechanisms in CMOS Downconverters," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 3, pp. 394–406, March 2003.

[59] Chehrazi, S. and Mirzaei, A. and Abidi, A.A., "Second-Order Intermodulation in Current-Commutating Passive FET Mixers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 12, pp. 2556–2568, Dec. 2009.

[60] M. J. M. Pelgrom and A. C. J. Duinmaijer, "Matching properties of mos transistors," in *Solid-State Circuits Conference, 1988. ESSCIRC '88. Fourteenth European*, 1988, pp. 327–330.

[61] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. Welbers, "Matching properties of mos transistors," *Solid-State Circuits, IEEE Journal of*, vol. 24, no. 5, pp. 1433–1439, 1989.

[62] Z. Ru, N. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally Enhanced Software-Defined Radio Receiver Robust to Out-of-Band Interference," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 12, pp. 3359–3375, Dec.

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This dissertation was typeset with LaTeX[†] by the author.

[†]LaTeX is a document preparation system developed by Leslie Lamport as a special version of Donald Knuth's TeX Program.